PEARSON

Power Electronics

Circuits, Devices, and Applications

Third Edition

Muhammad H. Rashid

Contents

Preface

The third edition of *Power Electronics* is intended as a textbook for a course on power electronics/static power converters for junior or senior undergraduate students in electrical and electronic engineering. It can also be used as a textbook for graduate students and as a reference book for practicing engineers involved in the design and applications of power electronics. The prerequisites are courses on basic electronics and basic electrical circuits. The content of *Power Electronics* is beyond the scope of a one-semester course. The time allocated to a course on power electronics in a typical undergraduate curriculum is normally only one semester. Power electronics has already advanced to the point where it is difficult to cover the entire subject in a one-semester course. For an undergraduate course, Chapters 1 to 11 should be adequate to provide a good background on power electronics. Chapters 12 to 16 could be left for other courses or included in a graduate course. Table P.1 shows suggested topics for a one-semester course on "Power Electronics" and Table P.2 for one semester course on "Power Electronics and Motor Drives."

TABLE P.1 Suggested Topics for One Semester Course on Power Electronics

Chapter	Topics	Sections	Lectures
1	Introduction	1.1 to 1.12	2
2	Power semiconductor diodes and circuits	2.1 to 2.4, 2.7, 2.10 to 2.13	2
3	Diode rectifiers	3.1 to 3.9	5
4	Power transistors	4.2, 4.10, 4.11	2
5	DC–DC converters	5.1 to 5.7	5
6	PWM inverters	6.1 to 6.6, 6.8 to 6.11	7
7	Thyristors	7.1 to 7.5, 7.9, 7.10	2
8	Resonant pulse inverters	8.1 to 8.5	3
10	Controlled rectifiers	10.1 to 10.6	6
11	AC voltage controllers	11.1 to 11.5	3
12	Static switches	12.1 to 12.8	2
	Mid-term exams and quizzes		3
	Final exam		3
	Total lectures in a 15-week semester		45

TABLE P.2 Suggested Topics for One Semester Course on Power Electronics and Motor Drives

Chapter	Topics	Sections	Lectures
1	Introduction	1.1 to 1.12	2
2	Power semiconductor diodes and circuits	2.1 to 2.4, 2.7, 2.10 to 2.13	2
3	Diode rectifiers	3.1 to 3.8	4
4	Power transistors	4.2, 4.10, 4.11	1
5	DC–DC converters	5.1 to 5.7	4
6	PWM inverters	6.1 to 6.6, 6.8 to 6.11	5
7	Thyristors	7.1 to 7.5, 7.9, 7.10	1
10	Controlled rectifiers	10.1 to 10.7	5
11	AC voltage controllers	11.1 to 11.5	2
Appendix	Magnetic circuits	B 1.6 to 16.6	1
15	DC drives	15.1 to 15.7	5
Appendix	Three-phase circuits	A 1.6 to 16.6	1
14	AC drives	16.1 to 16.6	6
	Mid-term exams and quizzes		3
	Final exam		3
	Total lectures in a 15-week semester		45

The fundamentals of power electronics are well established and they do not change rapidly. However, the device characteristics are continuously being improved and new devices are added. *Power Electronics*, which employs the bottom-up approach, covers device characteristics conversion techniques first and then applications. It emphasizes the fundamental principles of power conversions. This third edition of *Power Electronics* is a complete revision of the second edition, and (i) features bottom-up approach rather than top-down approach; (ii) introduces the state-of-the-art advanced Modulation Techniques; (iii) presents three new chapters on "Multilevel Inverters" (Chapter 9), "Flexible AC Transmission Systems" (Chapter 13), and "Gate Drive Circuits" (Chapter 17) and covers state-of-the-art techniques; (iv) integrates the industry standard software, SPICE, and design examples that are verified by SPICE simulation; (v) examines converters with RL-loads under both continuous and discontinuous current conduction; and (vi) has expanded sections and/or paragraphs to add explanations. The book is divided into five parts:

1. Introduction—Chapter 1
2. Devices and gate-drive circuits—Chapters 2, 4, 7, and 17
3. Power conversion techniques—Chapters 3, 5, 6, 8, 9, 10, and 11
4. Applications—Chapters 12, 13, 14, 15, and 16
5. Protection and thermal modeling—Chapter 18

Topics like three-phase circuits, magnetic circuits, switching functions of converters, DC transient analysis, and Fourier analysis are reviewed in the Appendices.

Power electronics deals with the applications of solid-state electronics for the control and conversion of electric power. Conversion techniques require the switching on and off of power semiconductor devices. Low-level electronics circuits, which normally consist of integrated circuits and discrete components, generate the required

gating signals for the power devices. Integrated circuits and discrete components are being replaced by microprocessors and signal processing ICs.

An ideal power device should have no switching-on and -off limitations in terms of turn-on time, turn-off time, current, and voltage handling capabilities. Power semiconductor technology is rapidly developing fast switching power devices with increasing voltage and current limits. Power switching devices such as power BJTs, power MOSFETs, SITs, IGBTs, MCTs, SITHs, SCRs, TRIACs, GTOs, MTOs, ETOs, IGCTs, and other semiconductor devices are finding increasing applications in a wide range of products. With the availability of faster switching devices, the applications of modern microprocessors and digital signal processing in synthesizing the control strategy for gating power devices to meet the conversion specifications are widening the scope of power electronics. The power electronics revolution has gained momentum, since the early 1990s. Within the next 20 years, power electronics will shape and condition the electricity somewhere between its generation and all its users. The potential applications of power electronics are yet to be fully explored but we've made every effort to cover as many applications as possible in this book.

Any comments and suggestions regarding this book are welcomed and should be sent to the author.

Dr. Muhammad H. Rashid
Professor and Director
Electrical and Computer Engineering
University of West Florida
11000 University Parkway
Pensacola, FL 32514–5754

E-mail: mrashid@uwf.edu

PSPICE SOFTWARE AND PROGRAM FILES

The student version PSpice schematics and/or Orcad capture software can be obtained or downloaded from

Cadence Design Systems, Inc.
2655 Seely Avenue
San Jose, CA 95134

Websites: http://www.cadence.com
http://www.orcad.com
http://www.pspice.com

The website http://uwf.edu/mrashid contains all PSpice circuits, PSpice schematics, Orcad capture, and Mathcad files for use with this book.

Important Note: The PSpice circuit files (with an extension .CIR) are self-contained and each file contains any necessary device or component models. However, the PSpice schematic files (with an extension .SCH) need the user-defined model library file ***Rashid_PE3_MODEL.LIB***, which is included with the schematic files, and ***must be included*** from the Analysis menu of PSpice Schematics. Similarly, the Orcad

schematic files (with extensions .OPJ and .DSN) need the user-defined model library file ***Rashid_PE3_MODEL.LIB***, which is included with the Orcad schematic files, ***must be included*** from the PSpice Simulation settings menu of Orcad Capture. Without these files being included while running the simulation, it will not run and will give errors.

ACKNOWLEDGMENTS

Many people have contributed to this edition and made suggestions based on their classroom experience as a professor or a student. I would like to thank the following persons for their comments and suggestions:

Mazen Abdel-Salam, *King Fahd University of Petroleum and Minerals, Saudi Arabia*
Johnson Asumadu, *Western Michigan University*
Ashoka K. S. Bhat, *University of Victoria, Canada*
Fred Brockhurst, *Rose-Hulman Institution of Technology*
Jan C. Cochrane, *The University of Melbourne, Australia*
Ovidiu Crisan, *University of Houston*
Joseph M. Crowley, *University of Illinois, Urbana-Champaign*
Mehrad Ehsani, *Texas A&M University*
Alexander E. Emanuel, *Worcester Polytechnic Institute*
George Gela, *Ohio State University*
Herman W. Hill, *Ohio University*
Constantine J. Hatziadoniu, *Southern Illinois University, Carbondale*
Wahid Hubbi, *New Jersey Institute of Technology*
Marrija Ilic-Spong, *University of Illinois, Urbana-Champaign*
Shahidul I. Khan, *Concordia University, Canada*
Hussein M. Kojabadi, *Sahand University of Technology , Iran*
Peter Lauritzen, *University of Washington*
Jack Lawler, *University of Tennessee*
Arthur R. Miles, *North Dakota State University*
Medhat M. Morcos, *Kansas State University*
Hassan Moghbelli, *Purdue University Calumet*
H. Rarnezani-Ferdowsi, *University of Mashhad, Iran*
Prasad Enjeti, *Texas A&M University*
Saburo Mastsusaki, *TDK Corporation, Japan*
Vedula V. Sastry, *Iowa State University*
Elias G. Strangas, *Michigan State University*
Selwyn Wright, *The University of Huddersfield, Queensgate, UK*
S. Yuvarajan, *North Dakota State University*

It has been a great pleasure working with the editor, Alice Dworkin and the production editor, Donna King. Finally, I would thank my family for their love, patience, and understanding.

MUHAMMAD H. RASHID
Pensacola, Florida

About the Author

Muhammad H. Rashid received the B.Sc. degree in electrical engineering from the Bangladesh University of Engineering and Technology and the M.Sc. and Ph.D. degrees from the University of Birmingham, UK.

Currently, he is a Professor of electrical engineering with the University of Florida and the Director of the UF/UWF Joint Program in Electrical and Computer Engineering. Previously, he was a Professor of electrical engineering and the Chair of the Engineering Department at Indiana University–Purdue University at Fort Wayne. In addition, he was a Visiting Assistant Professor of electrical engineering at the University of Connecticut, Associate Professor of electrical engineering at Concordia University (Montreal, Canada), Professor of electrical engineering at Purdue University, Calumet, and Visiting Professor of electrical engineering at King Fahd University of Petroleum and Minerals, Saudi Arabia. He has also been employed as a design and development engineer with Brush Electrical Machines Ltd. (UK), as a Research Engineer with Lucas Group Research Centre (UK), and as a Lecturer and Head of Control Engineering Department at the Higher Institute of Electronics (Malta). He is actively involved in teaching, researching, and lecturing in power electronics. He has published 14 books and more than 100 technical papers. His books have been adopted as textbooks all over the world. His book *Power Electronics* has been translated into Spanish, Portuguese, Indonesian, Korean and Persian. His book *Microelectronics* has been translated into Spanish in Mexico and Spain. He has had many invitations from foreign governments and agencies to be a keynote lecturer and consultant, from foreign universities to serve as an external Ph.D. examiner, and from funding agencies to serve as a research proposal reviewer. His contributions in education have been recognized by foreign governments and agencies. He has previously lectured and consulted for NATO for Turkey in 1994, UNDP for Bangladesh in 1989 and 1994, Saudi Arabia in 1993, Pakistan in 1993, Malaysia in 1995 and 2002, and Bangkok in 2002, and has been invited by foreign universities in Australia, Canada, Hong Kong, India, Malaysia, Singapore to serve as an external examiner for undergraduate, master's and Ph.D. degree examinations, by funding agencies in Australia, Canada, United States, and Hong Kong to review research proposals, and by U.S. and foreign universities to evaluate promotion cases for professorship. He has previously authored seven books published by Prentice Hall: *Power Electronics—Circuits, Devices, and Applications* (1988, 2/e 1993), *SPICE For Power Electronics* (1993), *SPICE for Circuits and Electronics Using PSpice*

(1990, 2/e 1995), *Electromechanical and Electrical Machinery* (1986), and *Engineering Design for Electrical Engineers* (1990). He has authored five IEEE self-study guides: *Self-Study Guide on Fundamentals of Power Electronics, Power Electronics Laboratory Using PSpice, Selected Readings on SPICE Simulation of Power Electronics*, and *Selected Readings on Power Electronics* (IEEE Press, 1996) and *Microelectronics Laboratory Using Electronics Workbench* (IEEE Press, 2000). He also wrote two books: *Electronic Circuit Design using Electronics Workbench* (January 1998), and *Microelectronic Circuits—Analysis and Design* (April 1999) by PWS Publishing). He is editor of *Power Electronics Handbook* published by Academic Press, 2001.

Dr. Rashid is a registered Professional Engineer in the Province of Ontario (Canada), a registered Chartered Engineer (UK), a Fellow of the Institution of Electrical Engineers (IEE, UK) and a Fellow of the Institute of Electrical and Electronics Engineers (IEEE, USA). He was elected as an IEEE Fellow with the citation "*Leadership in power electronics education and contributions to the analysis and design methodologies of solid-state power converters.*" He was the recipient of the *1991 Outstanding Engineer Award* from The Institute of Electrical and Electronics Engineers (IEEE). He received the 2002 IEEE Educational Activity Award (EAB) Meritorious Achievement Award in Continuing Education with the citation "*for contributions to the design and delivery of continuing education in power electronics and computer-aided-simulation*". He was also an ABET program evaluator for electrical engineering from 1995 to 2000 and he is currently an engineering evaluator for the Southern Association of Colleges and Schools (SACS, USA). He has been elected as an IEEE-Industry Applications Society (IAS) Distinguished Lecturer. He is the Editor-in-Chief of the *Power Electronics and Applications Series*, published by CRC Press.

CHAPTER 1

Introduction

The learning objectives of this chapter are as follows:

- To get an overview of power electronics and its history of development
- To get an overview of different types of power semiconductor devices and their switching characteristics
- To learn about the types of power converters
- To know about resources for finding manufacturers of power semiconductors
- To know about resources for finding published articles of power electronics and applications

1.1 APPLICATIONS OF POWER ELECTRONICS

The demand for control of electric power for electric motor drive systems and industrial controls existed for many years, and this led to early development of the Ward–Leonard system to obtain a variable dc voltage for the control of dc motor drives. Power electronics have revolutionized the concept of power control for power conversion and for control of electrical motor drives.

Power electronics combine power, electronics, and control. Control deals with the steady-state and dynamic characteristics of closed-loop systems. Power deals with the static and rotating power equipment for the generation, transmission, and distribution of electric energy. Electronics deal with the solid-state devices and circuits for signal processing to meet the desired control objectives. *Power electronics* may be defined as the applications of solid-state electronics for the control and conversion of electric power. The interrelationship of power electronics with power, electronics, and control is shown in Figure 1.1.

Power electronics are based primarily on the switching of the power semiconductor devices. With the development of power semiconductor technology, the power-handling capabilities and the switching speed of the power devices have improved tremendously. The development of microprocessors and microcomputer technology has a great impact on the control and synthesizing the control strategy for the power semiconductor devices. Modern power electronics equipment uses (1) power semiconductors that can be regarded as the muscle, and (2) microelectronics that have the power and intelligence of a brain.

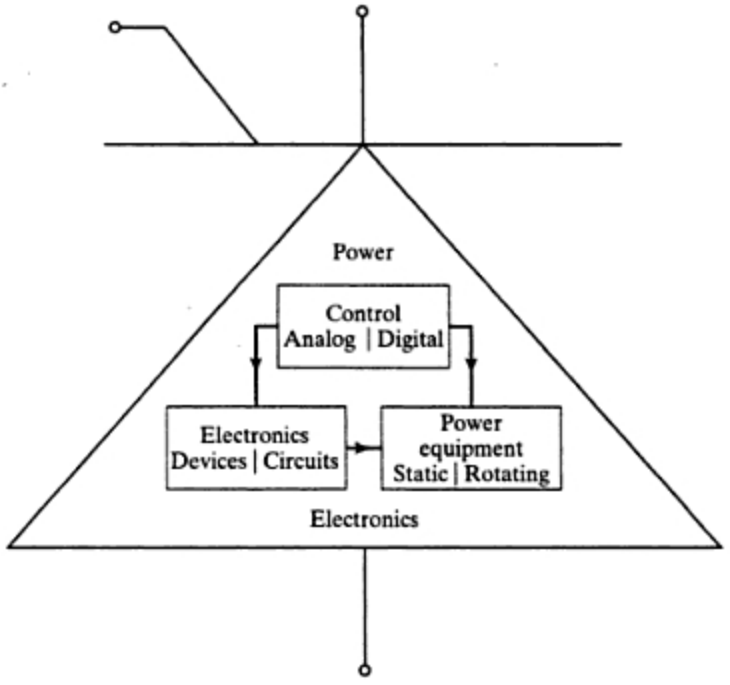


FIGURE 1.1

Relationship of power electronics to power, electronics, and control.

Power electronics have already found an important place in modern technology and are now used in a great variety of high-power products, including heat controls, light controls, motor controls, power supplies, vehicle propulsion systems, and high-voltage direct-current (HVDC) systems. It is difficult to draw the flexible ac transmissions (FACTs) boundaries for the applications of power electronics, especially with the present trends in the development of power devices and microprocessors. Table 1.1 shows some applications of power electronics [5].

1.1.1 History of Power Electronics

The history of power electronics began with the introduction of the mercury arc rectifier in 1900. Then the metal tank rectifier, grid-controlled vacuum-tube rectifier, ignitron, phanotron, and thyratron were introduced gradually. These devices were applied for power control until the 1950s.

The first electronics revolution began in 1948 with the invention of the silicon transistor at Bell Telephone Laboratories by Bardeen, Brattain, and Schockley. Most of today's advanced electronic technologies are traceable to that invention. Modern microelectronics evolved over the years from silicon semiconductors. The next breakthrough, in 1956, was also from Bell Laboratories: the invention of the *PNPN* triggering transistor, which was defined as a thyristor or silicon-controlled rectifier (SCR).

The second electronics revolution began in 1958 with the development of the commercial thyristor by the General Electric Company. That was the beginning of a

TABLE 1.1 Some Applications of Power Electronics

Advertising	Magnets
Air-conditioning	Mass transits
Aircraft power supplies	Mercury-arc lamp ballasts
Alarms	Mining
Appliances	Model trains
Audio amplifiers	Motor controls
Battery charger	Motor drives
Blenders	Movie projectors
Blowers	Nuclear reactor control rod
Boilers	Oil well drilling
Burglar alarms	Oven controls
Cement kiln	Paper mills
Chemical processing	Particle accelerators
Clothes dryers	People movers
Computers	Phonographs
Conveyors	Photocopies
Cranes and hoists	Photographic supplies
Dimmers	Power supplies
Displays	Printing press
Electric blankets	Pumps and compressors
Electric door openers	Radar/sonar power supplies
Electric dryers	Range surface unit
Electric fans	Refrigerators
Electric vehicles	Regulators
Electromagnets	RF amplifiers
Electromechanical electroplating	Security systems
Electronic ignition	Servo systems
Electrostatic precipitators	Sewing machines
Elevators	Solar power supplies
Fans	Solid-state contactors
Flashers	Solid-state relays
Food mixers	Space power supplies
Food warmer trays	Static circuit breakers
Forklift trucks	Static relays
Furnaces	Steel mills
Games	Synchronous machine starting
Garage door openers	Synthetic fibers
Gas turbine starting	Television circuits
Generator exciters	Temperature controls
Grinders	Timers
Hand power tools	Toys
Heat controls	Traffic signal controls
High-frequency lighting	Trains
High-voltage dc (HVDC)	TV deflections
Induction heating	Ultrasonic generators
Laser power supplies	Uninterruptible power supplies
Latching relays	Vacuum cleaners
Light dimmers	Volt-ampere reactive (VAR) compensation
Light flashers	Vending machines
Linear induction motor controls	Very low frequency (VLF) transmitters
Locomotives	Voltage regulators
Machine tools	Washing machines
Magnetic recordings	Welding

Source: Ref. 5.

FIGURE 1.2

History of power electronics. (Courtesy of Tennessee Center for Research and Development.)

new era of power electronics. Since then, many different types of power semiconductor devices and conversion techniques have been introduced. The microelectronics revolution gave us the ability to process a huge amount of information at incredible speed. The power electronics revolution is giving us the ability to shape and control large amounts of power with ever-increasing efficiency. Due to the marriage of power electronics, the muscle, with microelectronics, the brain, many potential applications of power electronics are now emerging, and this trend will continue. Within the next 30 years, power electronics will shape and condition the electricity somewhere in the transmission network between its generation and all its users. The power electronics revolution has gained momentum since the late 1980s and early 1990s [1]. A chronological history of power electronics is shown in Figure 1.2.

1.2 POWER SEMICONDUCTOR DEVICES

Since the first thyristor SCR was developed in late 1957, there have been tremendous advances in the power semiconductor devices. Until 1970, the conventional thyristors had been exclusively used for power control in industrial applications. Since 1970, various types of power semiconductor devices were developed and became commercially available. Figure 1.3 shows the classification of the power semiconductors, which are made of either silicon or silicon carbide. Silicon carbide devices are, however, under development. A majority of the devices are made of silicon. These devices can be divided broadly into three types: (1) power diodes, (2) transistors, and (3) thyristors. These can be divided broadly into five types: (1) power diodes, (2) thyristors, (3) power bipolar junction transistors (BJTs), (4) power metal oxide semiconductor field-effect transistors (MOSFETs), and (5) insulated-gate bipolar transistors (IGBTs) and static induction transistors (SITs).

1.2.1 Power Diodes

A diode has two terminals: a cathode and an anode. Power diodes are of three types: general purpose, high speed (or fast recovery), and Schottky. General-purpose diodes are available up to 6000 V, 4500 A, and the rating of fast-recovery diodes can go up to 6000 V, 1100 A. The reverse recovery time varies between 0.1 and 5 μs. The fast-recovery diodes are essential for high-frequency switching of power converters. Schottky diodes have low on-state voltage and very small recovery time, typically nanoseconds. The leakage current increases with the voltage rating and their ratings are limited to 100 V, 300 A. A diode conducts when its anode voltage is higher than that of the cathode; and the forward voltage drop of a power diode is very low, typically 0.5 and 1.2 V. If the cathode voltage is higher than its anode voltage, a diode is said to be in a *blocking mode*. Figure 1.4 shows various configurations of general-purpose diodes, which basically fall into two types. One is called a *stud*, or *stud-mounted* type, and the other is called a *disk, press pak*, or *hockey puck* type. In a stud-mounted type, either the anode or the cathode could be the stud.

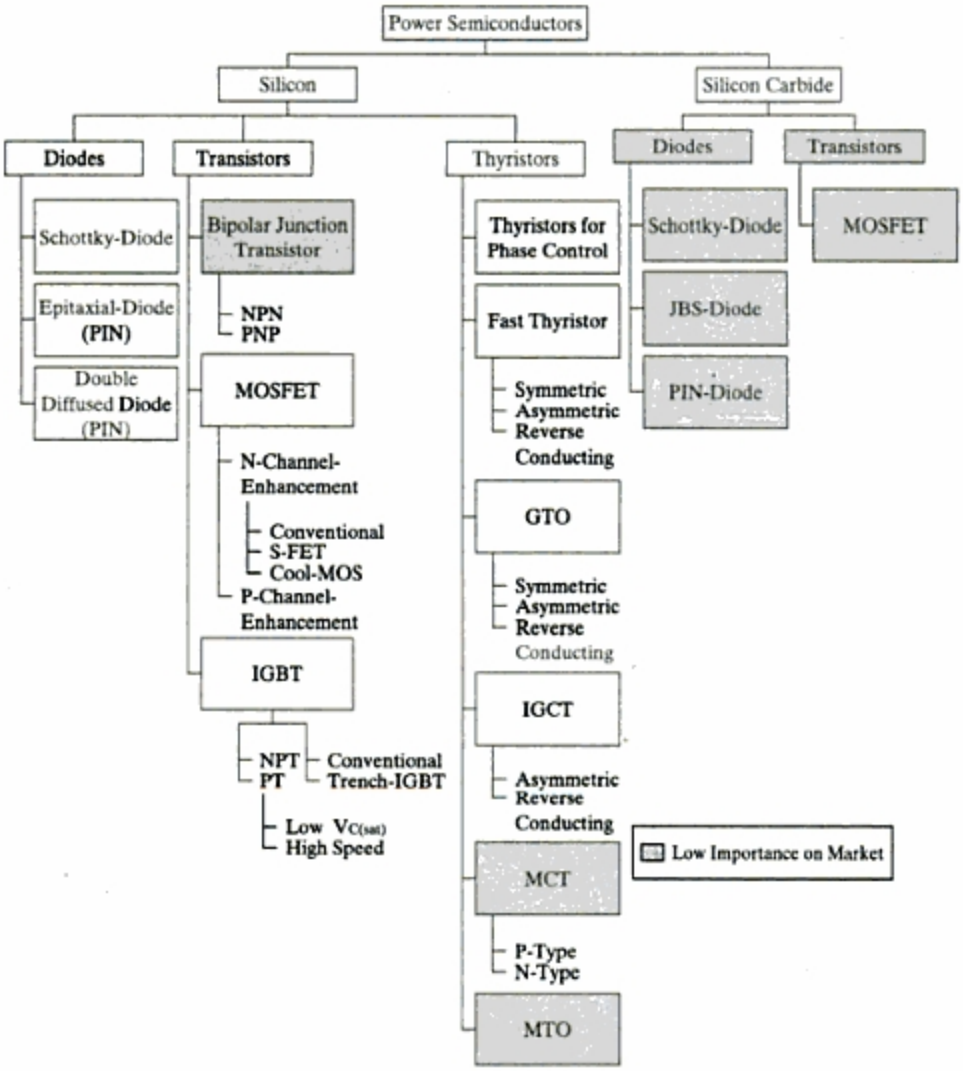


FIGURE 1.3

Classification of the power semiconductors. [Ref. 2, S. Bernet]

1.2.2 Thyristors

A thyristor has three terminals: an anode, a cathode, and a gate. When a small current is passed through the gate terminal to cathode, the thyristor conducts, provided that the anode terminal is at a higher potential than the cathode. The thyristors can be subdivided into eleven types: (a) forced-commutated thyristor, (b) line-commutated thyristor, (c) gate-turn-off thyristor (GTO), (d) reverse-conducting thyristor (RCT), (e) static induction thyristor (SITH), (f) gate-assisted turn-off thyristor (GATT), (g) light-activated silicon-controlled rectifier (LASCR), (h) MOS turn-off (MTO)

FIGURE 1.4

Various general-purpose diode configurations. (Courtesy of Powerex, Inc.)

thyristor, (i) emitter turn-off (ETO) thyristor, (j) integrated gate-commutated thyristor (IGCT), and (k) MOS-controlled thyristors (MCTs). Once a thyristor is in a conduction mode, the gate circuit has no control and the thyristor continues to conduct. When a thyristor is in a conduction mode, the forward voltage drop is very small, typically 0.5 to 2 V. A conducting thyristor can be turned off by making the potential of the anode equal to or less than the cathode potential. The line-commutated thyristors are turned off due to the sinusoidal nature of the input voltage, and forced-commutated thyristors are turned off by an extra circuit called *commutation circuitry*. Figure 1.5 shows various configurations of phase control (or line-commutated) thyristors: stud, hockey puck, flat, and pin types.

Natural or line-commutated thyristors are available with ratings up to 6000 V, 4500 A. The *turn-off time* of high-speed reverse-blocking thyristors has been improved substantially and it is possible to have 10 to 20 μs in a 3000-V, 3600-A thyristor. The turn-off time is defined as the time interval between the instant when the principal current has decreased to zero after external switching of the principal voltage circuit, and the instant when the thyristor is capable of supporting a specified principal voltage without

FIGURE 1.5

Various thyristor configurations. (Courtesy of Powerex, Inc.)

turning on. RCTs and GATTs are widely used for high-speed switching, especially in traction applications. An RCT can be considered as a thyristor with an inverse-parallel diode. RCTs are available up to 4000 V, 2000 A (and 800 A in reverse conduction) with a switching time of 40 μs. GATTs are available up to 1200 V, 400 A with a switching speed of 8 μs. LASCRs, which are available up to 6000 V, 1500 A, with a switching speed of 200 to 400 μs, are suitable for high-voltage power systems, especially in HVDC. For low-power ac applications, TRIACs are widely used in all types of simple heat controls, light controls, motor controls, and ac switches. The characteristics of TRIACs are similar to two thyristors connected in inverse parallel and having only one gate terminal. The current flow through a TRIAC can be controlled in either direction.

GTOs and SITHs are self-turned-off thyristors. GTOs and SITHs are turned on by applying a short positive pulse to the gates and are turned off by the applications of short negative pulse to the gates. They do not require any commutation circuit. GTOs are very attractive for forced commutation of converters and are available up to 6000 V, 6000 A. SITHs, whose ratings can go as high as 1200 V, 300 A, are expected to be applied for medium-power converters with a frequency of several hundred kilohertz and beyond the frequency range of GTOs. Figure 1.6 shows various configurations of GTOs. An MTO [3] is a combination of a GTO and a MOSFET, which together overcome the limitations of the GTO turn-off ability. Its structure is similar to that of a GTO and retains the GTO advantages of high voltage (up to 10 kV) and high current (up to 4000 A). MTOs can be used in high power applications ranging from 1 to 20 MVA. An ETO is a MOS-GTO hybrid device that combines the advantages of both the GTO and MOSFET. ETO has two gates: one normal gate for turn-on and one with a series MOSFET for turn-off. ETOs with a current rating of up to 4 kA and a voltage rating of up to 6 kV have been demonstrated.

An IGCT [4] integrates a gate-commutated thyristor (GCT) with a multilayered printed circuit board gate drive. The GCT is a hard-switched GTO with a very fast and large gate current pulse, as large as the full-rated current, that draws out all the current from the cathode into the gate in about 1 μs to ensure a fast turn-off. Similar to a GTO,

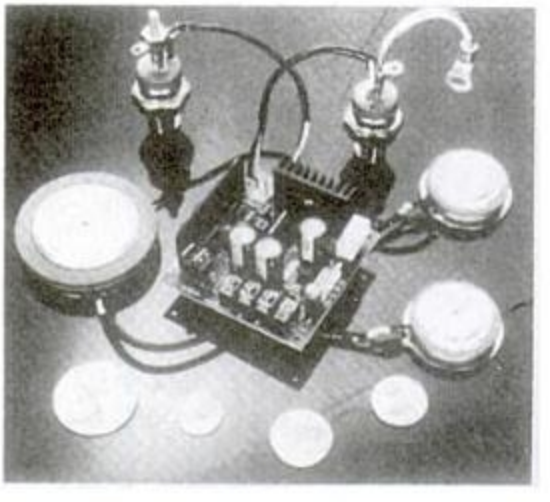


FIGURE 1.6

Gate-turn-off thyristors. (Courtesy of International Rectifiers.)

the IGCT is turned on by applying the turn-on current to its gate. The IGCT is turned off by a multilayered gate-driver circuit board that can supply a fast-rising turn-off pulse (i.e., a gate current of 4 kA/μs with gate-cathode voltage of 20 V only). An MCT can be turned "on" by a small negative voltage pulse on the MOS gate (with respect to its anode), and turned "off" by a small positive voltage pulse. It is like a GTO, except that the turn-off gain is very high. MCTs are available up to 4500 V, 250 A.

1.2.3 Power Transistors

Power transistors are of four types: (1) BJTs, (2) power MOSFETs, (3) IGBTs, and (4) SITs. A bipolar transistor has three terminals: base, emitter, and collector. It is normally operated as a switch in the common-emitter configuration. As long as the base of an *NPN*-transistor is at a higher potential than the emitter and the base current is sufficiently large to drive the transistor in the saturation region, the transistor remains on, provided that the collector-to-emitter junction is properly biased. High-power bipolar transistors are commonly used in power converters at a frequency below 10 kHz and are effectively applied in the power ratings up to 1200 V, 400 A. The various configurations of bipolar power transistors are shown in Figure 4.2. The forward drop of a conducting transistor is in the range 0.5 to 1.5 V. If the base drive voltage is withdrawn, the transistor remains in the nonconduction (or off) mode.

Power MOSFETs are used in high-speed power converters and are available at a relatively low power rating in the range of 1000 V, 100 A at a frequency range of several tens of kilohertz. The various power MOSFETs of different sizes are shown in Figure 4.24. IGBTs are voltage-controlled power transistors. They are inherently faster than BJTs, but still not quite as fast as MOSFETs. However, they offer far superior drive and output characteristics to those of BJTs. IGBTs are suitable for high voltage, high current, and frequencies up to 20 kHz. IGBTs are available up to 1700 V, 2400 A.

COOLMOS [8] is a new technology for high-voltage power MOSFETs, and it implements a compensation structure in the vertical drift region of a MOSFET to improve the on-state resistance. It has a lower on-state resistance for the same package compared with that of other MOSFETs. The conduction losses are at least 5 times less as compared with those of the conventional MOSFET technology. COOLMOS is capable of handling two to three times more output power as compared to the conventional MOSFET in the same package. The active chip area of COOLMOS is approximately 5 times smaller than that of a standard MOSFET. The on-state resistance of a 600 V, 47 A COOLMOS is 70 mΩ.

A SIT is a high-power, high-frequency device. It is essentially the solid-state version of the triode vacuum tube, and is similar to a junction field-effect transistor (JFET). It has a low-noise, low-distortion, high-audio-frequency power capability. The turn-on and turn-off times are very short, typically 0.25 μs. The normally on-characteristic and the high on-state drop limit its applications for general power conversions. The current rating of SITs can be up to 1200 V, 300 A, and the switching speed can be as high as 100 kHz. SITs are most suitable for high-power, high-frequency applications (e.g., audio, VHF/ultrahigh frequency [UHF], and microwave amplifiers).

Figure 1.7 shows the power range of commercially available power semiconductors. The ratings of commercially available power semiconductor devices are shown in Table 1.2, where the on-voltage is the on-state voltage drop of the device at

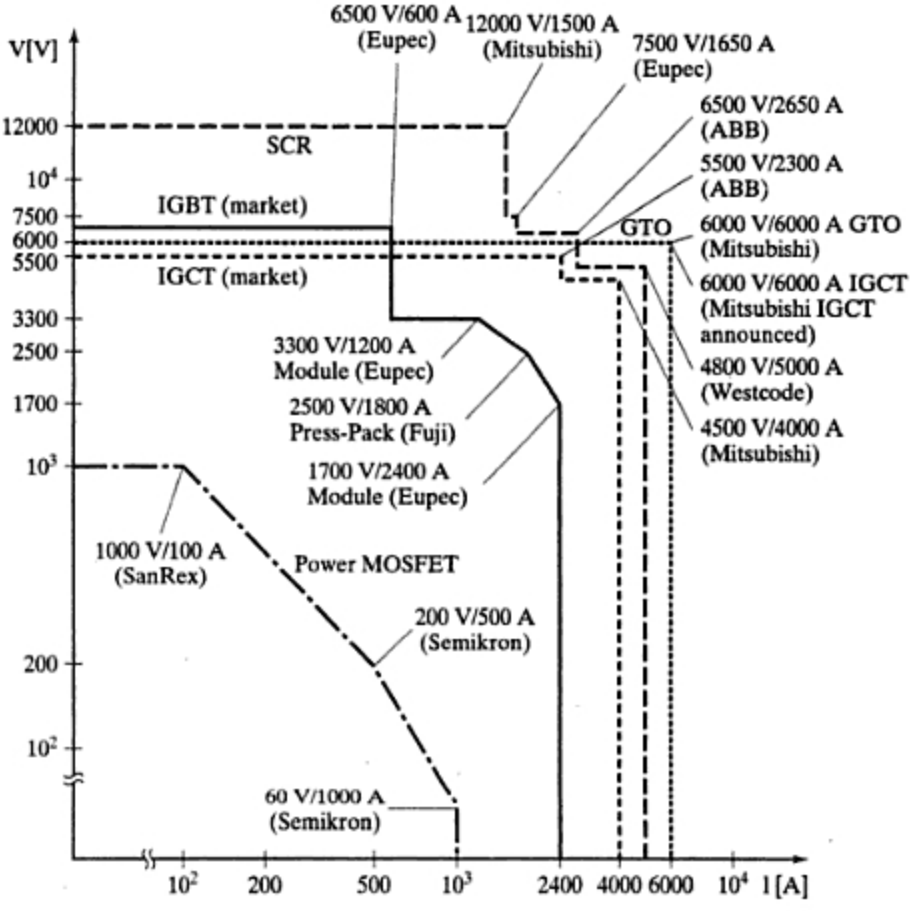


FIGURE 1.7

Power ranges of commercially available power semiconductors. [Ref. 2, S. Bernet]

the specified current. Table 1.3 shows the symbols and the $v-i$ characteristics of commonly used power semiconductor devices.

Figure 1.8 shows the applications and frequency range of power devices. A superpower device should (1) have a zero on-state voltage, (2) withstand an infinite off-state voltage, (3) handle an infinite current, and (4) turn on and off in zero time, thereby having infinite switching speed.

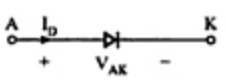
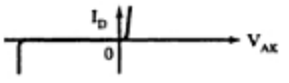
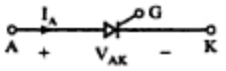
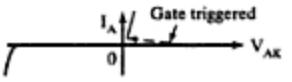
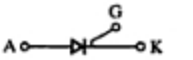
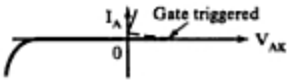
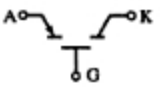
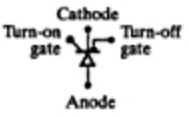
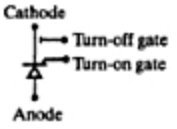
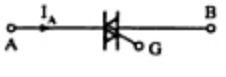
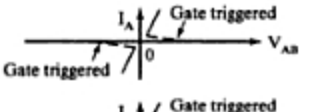
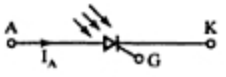
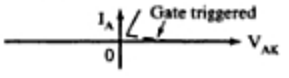
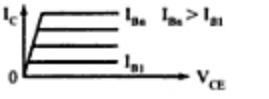
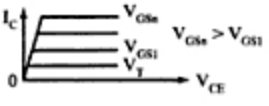
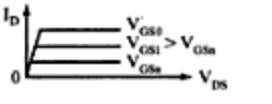
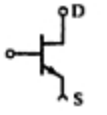
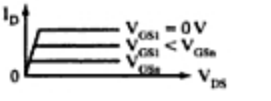
1.3 CONTROL CHARACTERISTICS OF POWER DEVICES

The power semiconductor devices can be operated as switches by applying control signals to the gate terminal of thyristors (and to the base of bipolar transistors). The required output is obtained by varying the conduction time of these switching devices. Figure 1.9 shows the output voltages and control characteristics of commonly used power switching devices. Once a thyristor is in a conduction mode, the gate signal of either positive or negative magnitude has no effect and this is shown in Figure 1.9a.

TABLE 1.2 Ratings of Power Semiconductor Devices

Device Type	Devices		Voltage/Current Rating	Upper Frequency (Hz)	Switching Time (μs)	On-State Resistance (Ω)
Power Diodes	Power diodes	General purpose	4000 V/4500 A	1 k	50–100	0.32 m
			6000 V/3500 A	1 k	50–100	0.6 m
			600 V/9570 A	1 k	50–100	0.1 m
			2800 V/1700 A	20 k	5–10	0.4 m
		High speed	4500 V/1950 A	20 k	5–10	1.2 m
			6000 V/1100 A	20 k	5–10	1.96 m
			600 V/17 A	30 k	0.2	0.14
		Schottky	150 V/80 A	30 k	0.2	8.63 m
Power Transistors	Bipolar transistors	Single	400 V/250 A	25 k	9	4 m
			400 V/40 A	30 k	6	31 m
			630 V/50 A	35 k	2	15 m
		Darlington	1200 V/400 A	20 k	30	10 m
	MOSFETs	Single	800 V/7.5 A	100 k	1.6	1
	COOLMOS	Single	800 V/7.8 A	125 k	2	1.2 m
			600 V/40 A	125 k	1	0.12 m
			1000 V/6.1 A	125 k	1.5	2 Ω
	IGBTs	Single	2500 V/2400 A	100 k	5–10	2.3 m
			1200 V/52 A	100 k	5–10	0.13
			1200 V/25 A	100 k	5–10	0.14
			1200 V/80 A	100 k	5–10	44 m
			1800 V/2200 A	100 k	5–10	1.76 m
	SITs		1200 V/300 A	100 k	0.5	1.2
Thyristors (Silicon-Controlled Rectifiers)	Phase control thyristors	Line-commutated low speed	6500 V/4200 A	60	100–400	0.58 m
			2800 V/1500 A	60	100–400	0.72 m
			5000 V/4600 A	60	100–400	0.48 m
			5000 V/3600 A	60	100–400	0.50 m
			5000 V/5000 A	60	100–400	0.45 m
	Forced-turned-off thyristors	Reverse blocking high speed	2800 V/1850 A	20 k	20–100	0.87 m
			1800 V/2100 A	20 k	20–100	0.78 m
			4500 V/3000 A	20 k	20–100	0.5 m
			6000 V/2300 A	20 k	20–100	0.52 m
			4500 V/3700 A	20 k	20–100	0.53 m
		Bidirectional	4200 V/1920 A	20 k	20–100	0.77 m
		RCT	2500 V/1000 A	20 k	20–100	2.1 m
		GATT	1200 V/400 A	20 k	10–50	2.2 m
		Light triggered	6000 V/1500 A	400	200–400	0.53 m
	Self-turned-off thyristors	GTO	4500 V/4000 A	10 k	50–110	1.07 m
		HD-GTO	4500 V/3000 A	10 k	50–110	1.07 m
		Pulse GTO	5000 V/4600 A	10 k	50–110	0.48 m
		SITH	4000 V/2200 A	20 k	5–10	5.6 m
		MTO	4500 V/500 A	5 k	80–110	10.2 m
		ETO	4500 V/4000 A	5 k	80–110	0.5 m
		IGCT	4500 V/3000 A	5 k	80–110	0.8 m
	TRIACs	Bidirectional	1200 V/300 A	400	200–400	3.6 m
	MCTs	Single	4500 V/250 A	5 k	50–110	10.4 m
			1400 V/65 A	5 k	50–110	28 m

TABLE 1.3 Characteristics and Symbols of Some Power Devices

Devices	Symbols	Characteristics
Diode		
Thyristor		
SITH		
GTO		
MCT		
MTO		
ETO		
IGCT		
TRIAC		
LASCR		
NPN BJT		
IGBT		
N-Channel MOSFET		
SIT		

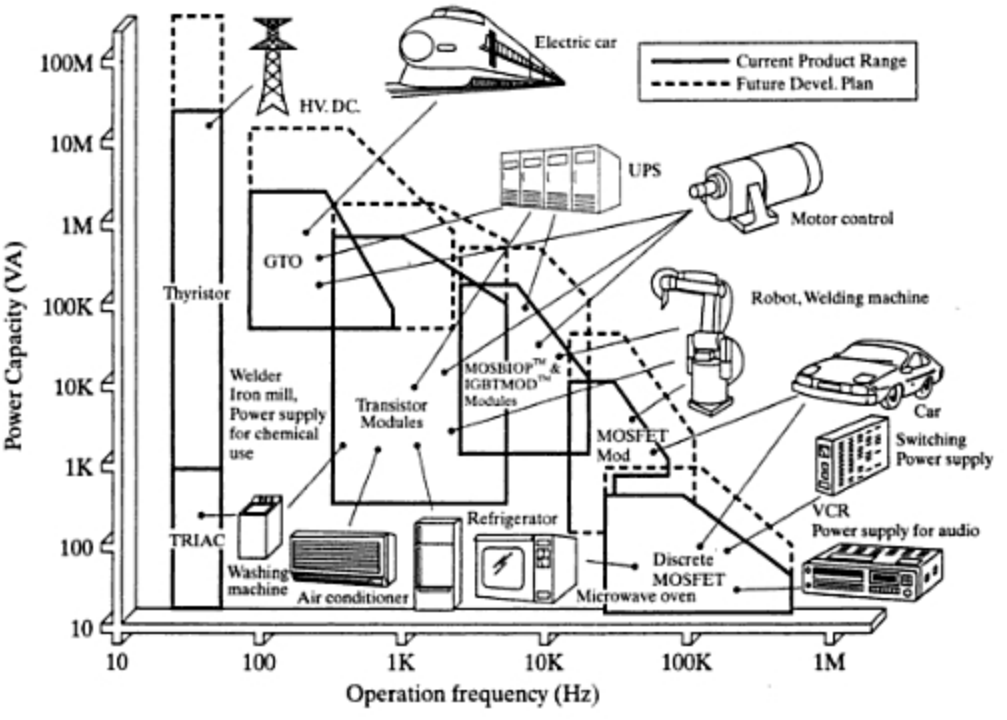


FIGURE 1.8

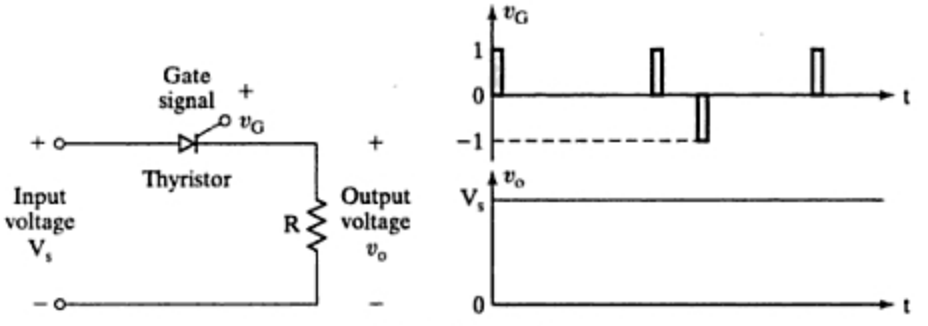
Applications of power devices. (Courtesy of Powerex, Inc.)

When a power semiconductor device is in a normal conduction mode, there is a small voltage drop across the device. In the output voltage waveforms in Figure 1.9, these voltage drops are considered negligible, and unless specified this assumption is made throughout the following chapters.

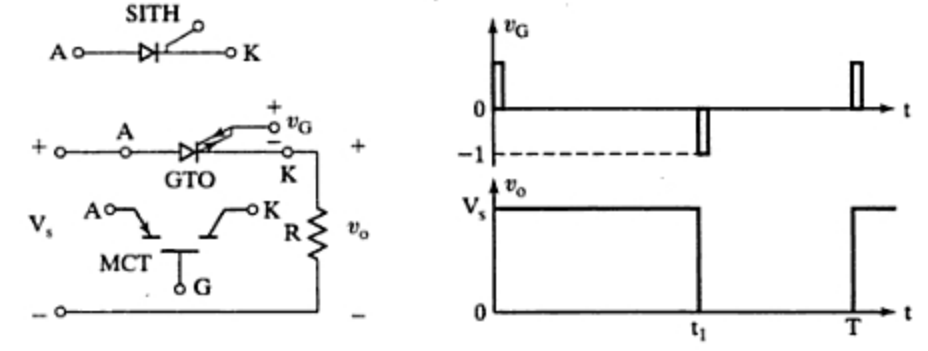
The power semiconductor switching devices can be classified on the basis of:

1. Uncontrolled turn on and off (e.g., diode);
2. Controlled turn on and uncontrolled turn off (e.g., SCR);
3. Controlled turn-on and -off characteristics (e.g., BJT, MOSFET, GTO, SITH, IGBT, SIT, MCT);
4. Continuous gate signal requirement (BJT, MOSFET, IGBT, SIT);
5. Pulse gate requirement (e.g., SCR, GTO, MCT);
6. Bipolar voltage-withstanding capability (SCR, GTO);
7. Unipolar voltage-withstanding capability (BJT, MOSFET, GTO, IGBT, MCT);
8. Bidirectional current capability (TRIAC, RCT);
9. Unidirectional current capability (SCR, GTO, BJT, MOSFET, MCT, IGBT, SITH, SIT, diode).

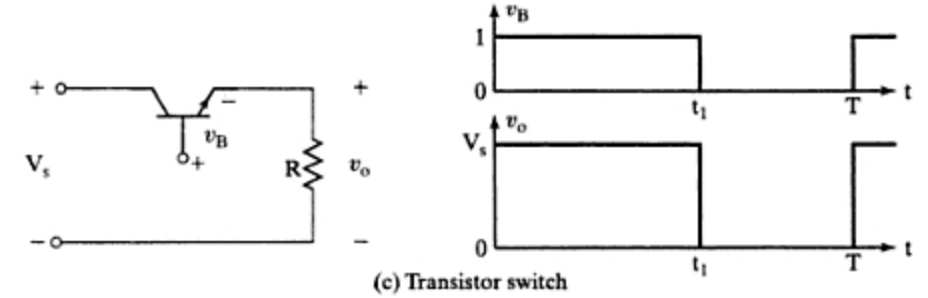
Table 1.4 shows the switching characteristics in terms of its voltage, current, and gate signals.



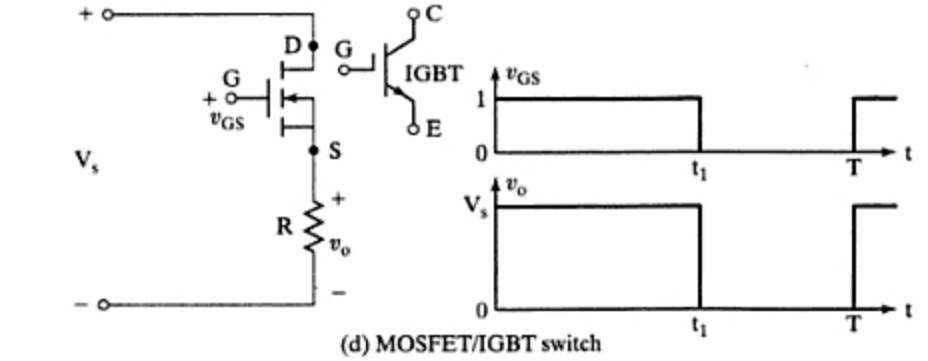
(a) Thyristor switch



(b) GTO/MTO/ETO/IGCT/MCT/SITH switch (For MCT, the polarity of V_G is reversed as shown)



(c) Transistor switch



(d) MOSFET/IGBT switch

FIGURE 1.9

Control characteristics of power switching devices.

TABLE 1.4 Switching Characteristics of Power Semiconductors

Device Type	Device	Continuous Gate	Pulse Gate	Controlled Turn-On	Controlled Turn-Off	Unipolar Voltage	Bipolar Voltage	Unidirectional Current	Bidirectional Current
Diodes	Power diode					x		x	
Transistors	BJT	x		x	x	x		x	
	MOSFET	x		x	x	x			x
	COOLMOS	x		x	x	x			x
	IGBT	x		x	x	x		x	
	SIT	x		x	x	x		x	
Thyristors	SCR		x	x			x	x	
	RCT		x	x			x		x
	TRIAC		x	x			x		x
	GTO		x	x	x		x	x	
	MTO		x	x	x		x	x	
	ETO		x	x	x		x	x	
	IGCT		x	x	x		x	x	
	SITH		x	x	x		x	x	
	MCT	x		x	x		x	x	

1.4 CHARACTERISTICS AND SPECIFICATIONS OF SWITCHES

There are many types of power switching devices. Each device, however, has its advantages and disadvantages and is suitable to specific applications. The motivation behind the development of any new device is to achieve the characteristics of a "super device." Therefore, the characteristics of any real device can be compared and evaluated with reference to the ideal characteristics of a super device.

1.4.1 Ideal Characteristics

The characteristics of an ideal switch are as follows:

1. In the on-state when the switch is on, it must have (a) the ability to carry a high forward current I_F, tending to infinity; (b) a low on-state forward voltage drop V_{ON}, tending to zero; and (c) a low on-state resistance R_{ON}, tending to zero. Low R_{ON} causes low on-state power loss P_{ON}. These symbols are normally referred to under dc steady-state conditions.
2. In the off-state when the switch is off, it must have (a) the ability to withstand a high forward or reverse voltage V_{BR}, tending to infinity; (b) a low off-state leakage current I_{OFF}, tending to zero; and (c) a high off-state resistance R_{OFF}, tending to infinity. High R_{OFF} cause low off-state power loss P_{OFF}. These symbols are normally referred to under dc steady-state conditions.
3. During the turn-on and turn-off process, it must be completely turned on and off instantaneously so that the device can be operated at high frequencies. Thus, it must have (a) a low delay time t_d, tending to zero; (b) a low rise time t_r, tending to zero; (c) a low storage time t_s, tending to zero; and (d) a low fall time t_f, tending to zero.
4. For turn-on and turn-off, it must require (a) a low gate-drive power P_G, tending to zero; (b) a low gate-drive voltage V_G, tending to zero; and (c) a low gate-drive current I_G, tending to zero.
5. Both turn-on and turn-off must be controllable. Thus, it must turn on with a gate signal (e.g., positive) and must turn off with another gate signal (e.g., zero or negative).
6. For turning on and off, it should require a pulse signal only, that is, a small pulse with a very small width t_W, tending to zero.
7. It must have a high dv/dt, tending to infinity. That is, the switch must be capable of handling rapid changes of the voltage across it.
8. It must have a high di/dt, tending to infinity. That is, the switch must be capable of handling a rapid rise of the current through it.
9. It requires very low thermal impedance from the internal junction to the ambient R_{JA}, tending to zero so that it can transmit heat to the ambient easily.
10. The ability to sustain any fault current for a long time is needed; that is, it must have a high value of i^2t, tending to infinity.

11. Negative temperature coefficient on the conducted current is required to result in an equal current sharing when the devices are operated in parallel.
12. Low price is a very important consideration for reduced cost of the power electronics equipment.

1.4.2 Characteristics of Practical Devices

During the turn-on and -off process, a practical switching device, shown in Figure 1.10a, requires a finite delay time (t_d), rise time (t_r), storage time (t_s), and fall time (t_f). As the device current i_{sw} rises during turn-on, the voltage across the device v_{sw} falls. As the device current falls during turn-off, the voltage across the device rises. The typical waveforms of device voltages v_{sw} and currents i_{sw} are shown in Figure 1.10b. The turn-on

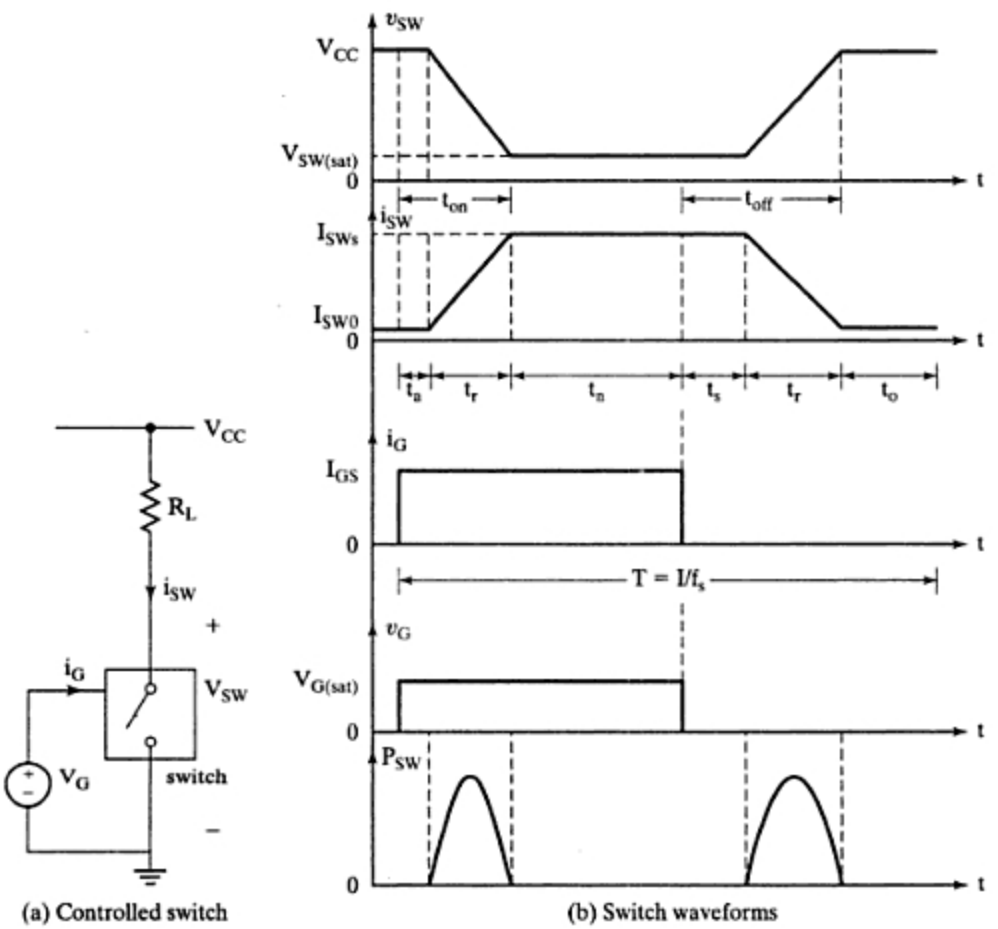


FIGURE 1.10

Typical waveforms of device voltages and currents.

time (t_{on}) of a device is the sum of the delay time and the rise time, whereas the turn-off time (t_{off}) of a device is the sum of the storage time and the fall time. In contrast to an ideal, lossless switch, a practical switching device dissipates some energy when conducting and switching. Voltage drop across a conducting power device is at least on the order of 1 V, but can often be higher, up to several volts. The goal of any new device is to improve the limitations imposed by the switching parameters.

The average conduction power loss, P_{ON} is given by

$$P_{ON} = \frac{1}{T_S}\int_0^{t_{ON}} p\,dt \tag{1.1}$$

where T_S denotes the conduction period and p is the instantaneous power loss (i.e., product of the voltage drop v_{sw} across the switch and the conducted current i_{sw}). Power losses increase during turn-on and turn-off of the switch because during the transition from one conduction state to another state both the voltage and current have significant values. The resultant switching power loss P_{SW} during the turn-on and turn-off periods, is given by

$$P_{SW} = f_s\left(\int_0^{t_r} p\,dt + \int_0^{t_s} p\,dt + \int_0^{t_f} p\,dt\right) \tag{1.2}$$

$f_S = 1/T_S$ is the switching frequency; t_r, t_s, and f_f are the rise time, storage time, and fall time respectively. Therefore, the power dissipation of a switching device is given by:

$$P_D = P_{ON} + P_{SW} + P_G \tag{1.3}$$

where P_G is the gate driver power.

1.4.3 Switch Specifications

The characteristics of practical semiconductor devices differ from those of an ideal device. The device manufacturers supply data sheets describing the device parameters and their ratings. There are many parameters that are important to the devices. The most important among these are:

Voltage ratings: Forward and reverse repetitive peak voltages, and an on-state forward voltage drop.

Current ratings: Average, root-mean-square (rms), repetitive peak, nonrepetitive peak, and off-state leakage currents.

Switching speed or frequency: Transition from a fully nonconducting to a fully conducting state (turn-on) and from a fully conducting to a fully nonconducting state (turn-off) are very important parameters. The switching period T_S and frequency f_S are given by

$$f_S = \frac{1}{T_S} = \frac{1}{t_d + t_r + t_{on} + t_s + t_f + t_{off}} \tag{1.4}$$

where t_{off} is the off time during which the switch remains off.

di/dt rating: The device needs a minimum amount of time before its whole conducting surface comes into play in carrying the full current. If the current rises rapidly, the current flow may be concentrated to a certain area and the device may be damaged. The *di/dt* of the current through the device is normally limited by connecting a small inductor in series with the device, known as a *series snubber.*

dv/dt rating: A semiconductor device has an internal junction capacitance C_J. If the voltage across the switch changes rapidly during turn-on, turn-off and also while connecting the main supply the initial current, the current $C_J\, dv/dt$ flowing through C_J may be too high, thereby causing damage to the device. The *dv/dt* of the voltage across the device is limited by connecting an *RC* circuit across the device, known as a *shunt snubber*, or simply *snubber.*

Switching losses: During turn-on the forward current rises before the forward voltage falls, and during turn-off the forward voltage rises before the current falls. Simultaneous existence of high voltage and current in the device represents power losses as shown in Figure 1.10b. Because of their repetitiveness, they represent a significant part of the losses, and often exceed the on-state conduction losses.

Gate drive requirements: The gate-drive voltage and current are important parameters to turn-on and -off a device. The gate-driver power and the energy requirement are very important parts of the losses and total equipment cost. With large and long current pulse requirements for turn-on and turn-off, the gate drive losses can be significant in relation to the total losses and the cost of the driver circuit can be higher than the device itself.

Safe operating area (SOA): The amount of heat generated in the device is proportional to the power loss, that is, the voltage-current product. For this product to be constant $P = vi$ and equal to the maximum allowable value, the current must be inverse proportional to the voltage. This yields the SOA limit on the allowable steady-state operating points in the voltage-current coordinates.

I^2t for fusing: This parameter is needed for fuse selection. The I^2t of the device must be less than that of the fuse so that the device is protected under fault current conditions.

Temperatures: Maximum allowable junction, case and storage temperatures, usually between 150°C and 200°C for junction and case, and between −50°C and 175°C for storage.

Thermal resistance: Junction-to-case thermal resistance, Q_{JC}; case-to-sink thermal resistance, Q_{CS}; and sink-ambient thermal resistance, Q_{SA}. Power dissipation must be rapidly removed from the internal wafer through the package and ultimately to the cooling medium. The size of semiconductor power switches is small, not exceeding 150 mm, and the thermal capacity of a bare device is too low to safely remove the heat generated by internal losses. Power devices are generally mounted on heat sinks. Thus, removing heat represents a high cost of equipment.

1.4.4 Device Choices

Although, there are many power semiconductor devices, none of them have the ideal characteristics. Continuous improvements are made to the existing devices and new

devices are under development. For high power applications from the ac 50- to 60-Hz main supply, the phase control and bidirectional thyristors are the most economical choices. COOLMOSs and IGBTs are the potential replacements for MOSFETS and BJTs, respectively, in low and medium power applications. GTOs and IGCTs are most suited for high-power applications requiring forced commutation. With the continuous advancement in technology, IGBTs are increasingly employed in high-power applications and MCTs may find potential applications that require bidirectional blocking voltages.

1.5 TYPES OF POWER ELECTRONIC CIRCUITS

For the control of electric power or power conditioning, the conversion of electric power from one form to another is necessary and the switching characteristics of the power devices permit these conversions. The static power converters perform these functions of power conversions. A converter may be considered as a switching matrix. The power electronics circuits can be classified into six types:

1. Diode rectifiers
2. Ac–dc converters (controlled rectifiers)
3. Ac–ac converters (ac voltage controllers)
4. Dc–dc converters (dc choppers)
5. Dc–ac converters (inverters)
6. Static switches

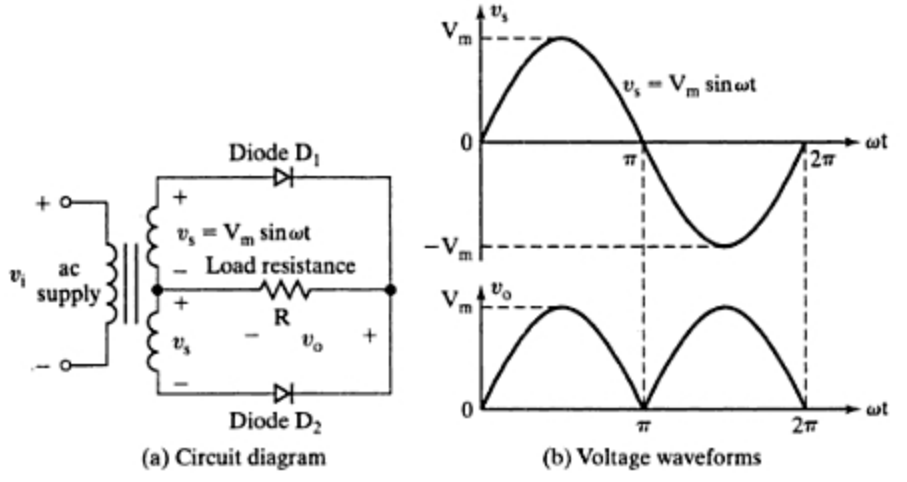
The devices in the following converters are used to illustrate the basic principles only. The switching action of a converter can be performed by more than one device. The choice of a particular device depends on the voltage, current, and speed requirements of the converter.

Diode Rectifiers. A diode rectifier circuit converts ac voltage into a fixed dc voltage and is shown in Figure 1.11. The input voltage to the rectifier v_i could be either single phase or three phase.

Ac–dc converters. A single-phase converter with two natural commutated thyristors is shown in Figure 1.12. The average value of the output voltage v_0 can be controlled by varying the conduction time of thyristors or firing delay angle, α. The input could be a single- or three-phase source. These converters are also known as *controlled rectifiers.*

Ac–ac converters. These converters are used to obtain a variable ac output voltage v_0 from a fixed ac source and a single-phase converter with a TRIAC is shown in Figure 1.13. The output voltage is controlled by varying the conduction time of a TRIAC or firing delay angle, α. These types of converters are also known as *ac voltage controllers.*

Dc–dc converters. A dc–dc converter is also known as a *chopper*, or *switching regulator*, and a transistor chopper is shown in Figure 1.14. The average output voltage v_o is controlled by varying the conduction time t, of transistor Q_1. If T is the chopping period, then $t_1 = \delta T$. δ is called as the *duty cycle* of the chopper.

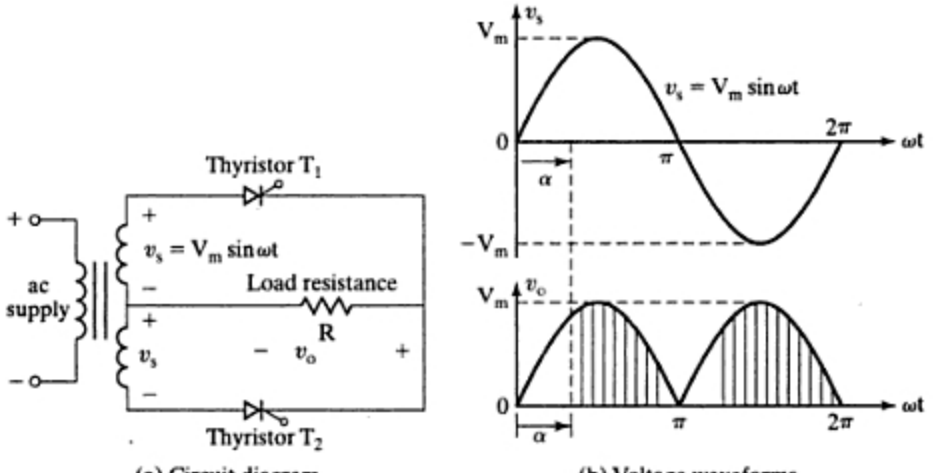


(a) Circuit diagram (b) Voltage waveforms

FIGURE 1.11

Single-phase diode rectifier circuit.

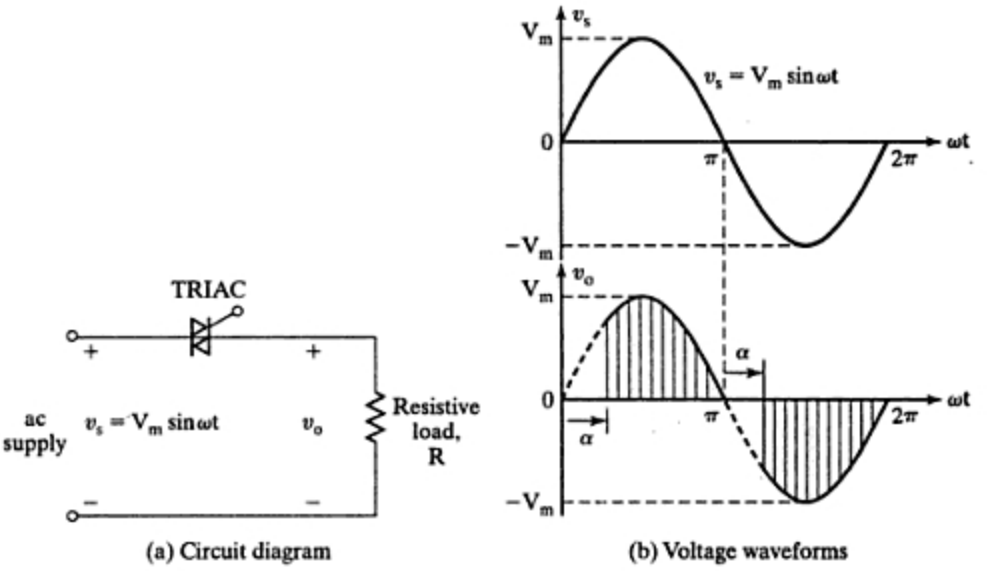
Dc–ac converters. A dc–ac converter is also known as an *inverter*. A single-phase transistor inverter is shown in Figure 1.15. If transistors M_1 and M_2 conduct for one half of a period and M_3 and M_4 conduct for the other half, the output voltage is of the alternating form. The output voltage can be controlled by varying the conduction time of transistors.



(a) Circuit diagram (b) Voltage waveforms

FIGURE 1.12

Single-phase ac–dc converter.



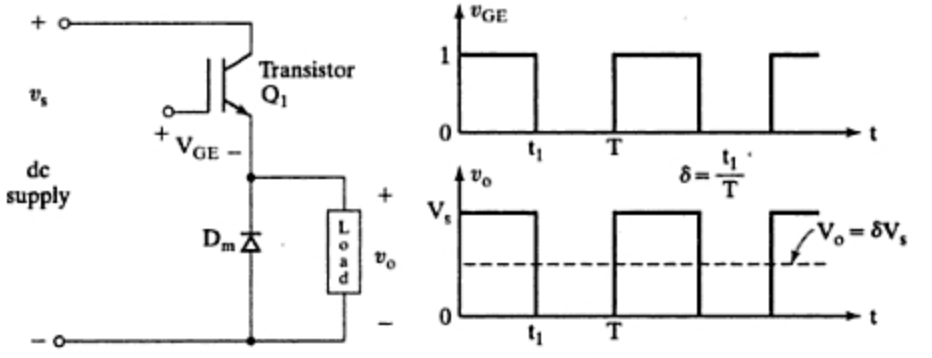
(a) Circuit diagram (b) Voltage waveforms

FIGURE 1.13

Single-phase ac–ac converter.

Static switches. Because the power devices can be operated as static switches or contactors, the supply to these switches could be either ac or dc and the switches are called as *ac static switches* or *dc switches*.

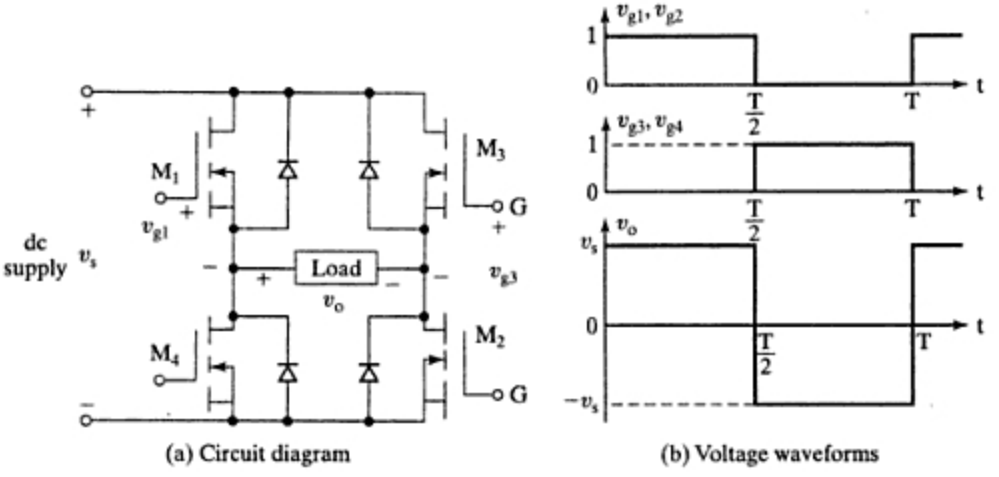
A number of conversion stages are often cascaded to produce the desired output as shown in Figure 1.16. Mains 1 supplies the normal ac supply to the load through the static bypass. The ac–dc converter charges the standby battery from mains 2. The dc–ac



(a) Circuit diagram (b) Voltage waveforms

FIGURE 1.14

Dc–dc converter.



(a) Circuit diagram (b) Voltage waveforms

FIGURE 1.15

Single-phase dc–ac converter.

converter supplies the emergency power to the load through an isolating transformer. Mains 1 and mains 2 are normally connected to the same ac supply.

1.6 DESIGN OF POWER ELECTRONICS EQUIPMENT

The design of a power electronics equipment can be divided into four parts:

1. Design of power circuits
2. Protection of power devices
3. Determination of control strategy
4. Design of logic and gating circuits

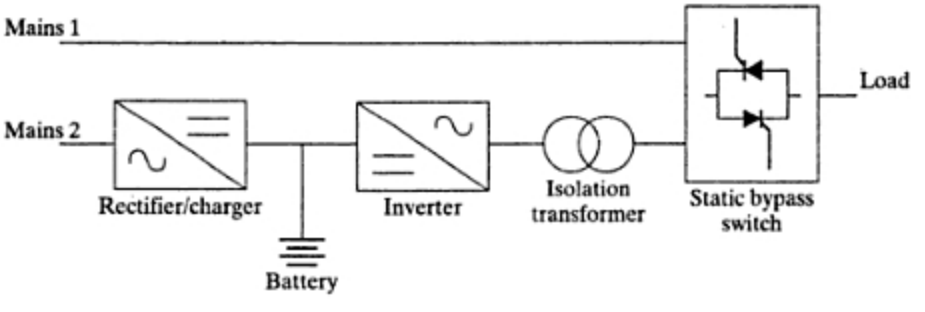


FIGURE 1.16

Block diagram of an uninterruptible power supply (UPS).

In the chapters that follow, various types of power electronic circuits are described and analyzed. In the analysis, the power devices are assumed to be ideal switches unless stated otherwise; and effects of circuit stray inductance, circuit resistances, and source inductance are neglected. The practical power devices and circuits differ from these ideal conditions and the designs of the circuits are also affected. However, in the early stage of the design, the simplified analysis of a circuit is very useful to understand the operation of the circuit and to establish the characteristics and control strategy.

Before a prototype is built, the designer should investigate the effects of the circuit parameters (and devices imperfections) and should modify the design if necessary. Only after the prototype is built and tested, the designer can be confident about the validity of the design and can estimate more accurately some of the circuit parameters (e.g., stray inductance).

1.7 DETERMINING THE ROOT-MEAN-SQUARE VALUES OF WAVEFORMS

To accurately determine the conduction losses in a device and the current ratings of the device and components, the rms values of the current waveforms must be known. The current waveforms are rarely simple sinusoids or rectangles, and this can pose some problems in determining the rms values. The rms value of a waveform $i(t)$ can be calculated as

$$I_{\text{rms}} = \sqrt{\frac{1}{T}\int_0^T i^2\,dt} \tag{1.5}$$

where T is the time period. If a waveform can be broken up into harmonics whose rms values can be calculated individually, the rms values of the actual waveform can be approximated satisfactorily by combining the rms values of the harmonics. That is, the rms value of the waveform can be calculated from

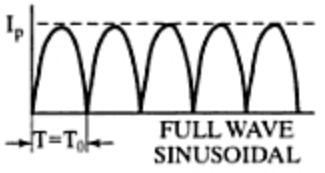
$$I_{\text{rms}} = \sqrt{I_{\text{dc}}^2 + I_{\text{rms}(1)}^2 + I_{\text{rms}(2)}^2 + \cdots + I_{\text{rms}(n)}^2} \tag{1.6}$$

where I_{dc} = the dc component. $I_{\text{rms}(1)}$ and $I_{\text{rms}(n)}$ are the rms values of the fundamental and nth harmonic components, respectively.

Figure 1.17 shows the rms values of different waveforms that are commonly encountered in power electronics.

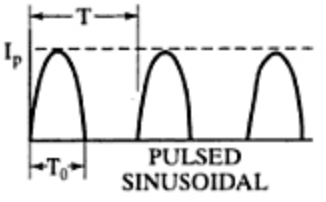
1.8 PERIPHERAL EFFECTS

The operations of the power converters are based mainly on the switching of power semiconductor devices; and as a result the converters introduce current and voltage harmonics into the supply system and on the output of the converters. These can cause problems of distortion of the output voltage, harmonic generation into the supply system, and interference with the communication and signaling circuits. It is normally necessary to introduce filters on the input and output of a converter system to reduce the



(a)

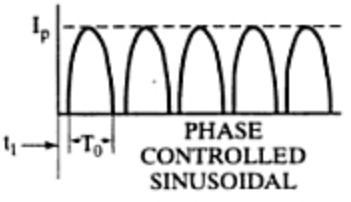
$$I_{RMS} = \frac{I_p}{\sqrt{2}}$$



(b)

$$I_{RMS} = I_p\sqrt{\frac{k}{2}}$$

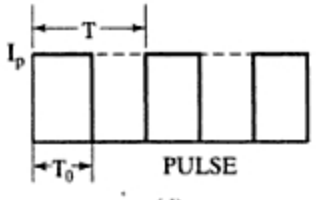
$$k = \frac{T_0}{T}$$



(c)

$$I_{RMS} = I_p\left[\frac{k}{2} + \frac{\sin T_0(1-k)\cos\pi(1-k)}{2\pi}\right]^{1/2}$$

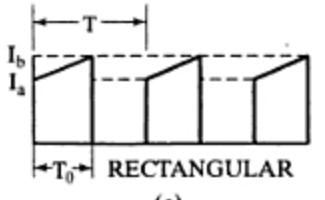
$$k = 1 - \frac{t_1}{T}$$



(d)

$$I_{RMS} = I_p\sqrt{k}$$

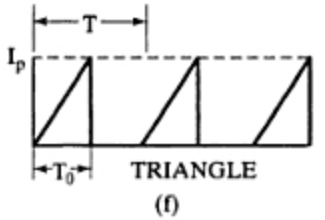
$$k = \frac{T_0}{T}$$



(e)

$$I_{RMS} = \left[k(I_b^2 + I_aI_b + I_a^2)/3\right]^{1/2}$$

$$k = \frac{T_0}{T}$$



(f)

$$I_{RMS} = I_p\sqrt{\frac{k}{3}}$$

$$k = \frac{T_0}{T}$$

FIGURE 1.17

The rms values of commonly encountered waveforms.

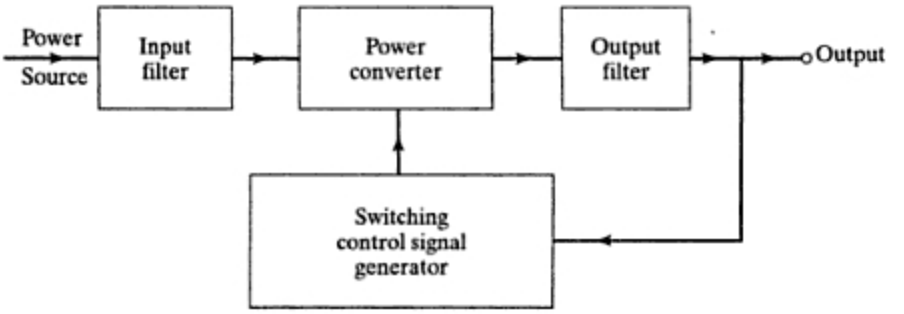


FIGURE 1.18

Generalized power converter system.

harmonic level to an acceptable magnitude. Figure 1.18 shows the block diagram of a generalized power converter. The application of power electronics to supply the sensitive electronic loads poses a challenge on the power quality issues and raises problems and concerns to be resolved by researchers. The input and output quantities of converters could be either ac or dc. Factors such as total harmonic distortion (THD), displacement factor (DF), and input power factor (IPF) are measures of the quality of a waveform. To determine these factors, finding the harmonic content of the waveforms is required. To evaluate the performance of a converter, the input and output voltages and currents of a converter are expressed in a Fourier series. The quality of a power converter is judged by the quality of its voltage and current waveforms.

The control strategy for the power converters plays an important part on the harmonic generation and output waveform distortion, and can be aimed to minimize or reduce these problems. The power converters can cause radio-frequency interference due to electromagnetic radiation, and the gating circuits may generate erroneous signals. This interference can be avoided by *grounded shielding.*

1.9 POWER MODULES

Power devices are available as a single unit or in a module. A power converter often requires two, four, or six devices, depending on its topology. Power modules with dual (in half-bridge configuration) or quad (in full bridge) or six (in three phase) are available for almost all types of power devices. The modules offer the advantages of lower on-state losses, high voltage and current switching characteristics, and higher speed than that of conventional devices. Some modules even include transient protection and gate drive circuitry.

1.10 INTELLIGENT MODULES

Gate drive circuits are commercially available to drive individual devices or modules. *Intelligent modules*, which are the state-of-the-art power electronics, integrate the power module and the peripheral circuit. The peripheral circuit consists of input or

output isolation from, and interface with, the signal and high-voltage system, a drive circuit, a protection and diagnostic circuit (against excess current, short circuit, an open load, overheating, and an excess voltage), microcomputer control, and a control power supply. The users need only to connect external (floating) power supplies. An intelligent module is also known as *smart power*. These modules are used increasingly in power electronics [6]. Smart power technology can be viewed as a box that interfaces power source to any load. The box interface function is realized with high-density complementary metal oxide semiconductor (CMOS) logic circuits, its sensing and protection function with bipolar analog and detection circuits, and its power control function with power devices and their associated drive circuits. The functional block diagram of a smart power system [7] is shown in Figure 1.19.

The analog circuits are used for creating the sensors necessary for self-protection and for providing a rapid feedback loop, which can terminate chip operation harmlessly when the system conditions exceed the normal operating conditions. For example, smart power chips must be designed to shut down without damage when a short circuit occurs across a load such as a motor winding. With smart power technology, the load current is monitored, and whenever this current exceeds a preset limit, the drive voltage to the power switches is shut off. In addition to this over-current protection features such as

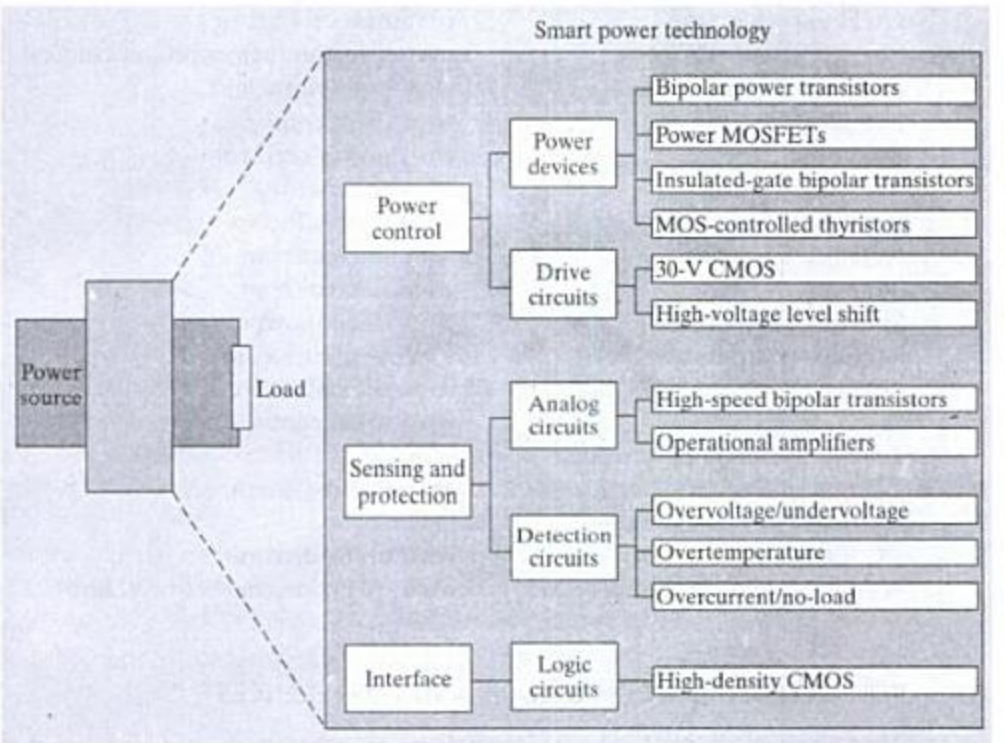


FIGURE 1.19

Functional block diagram of a smart power. [Ref. 7, J. Baliga]

overvoltage and overtemperature protection are commonly included to prevent destructive failures. Some manufacturers of devices and modules and their Web sites are as follows:

Advanced Power Technology, Inc.	www.advancedpower.com/
ABB Semiconductors	www.abbsem.com/
Eupec	www.eupec.com/p/index.htm
Fuji Electric	www.fujielectric.co.jp/eng/denshi/scd/index.htm
Collmer Semiconductor, Inc.	www.collmer.com
Dynex Semiconductor	www.dynexsemi.com
Harris Corp.	www.harris.com/
Hitachi, Ltd. Power Devices	www.hitachi.co.jp/pse
Infineon Technology	www.infineon.com/
International Rectifier	www.irf.com
Marconi Electronic Devices, Inc.	www.marconi.com/
Mitsubishi Semiconductors	www.mitsubishielectric.com/
Mitel Semiconductors	www.mitelsemi.com
Motorola, Inc.	www.motorola.com
National Semiconductors, Inc.	www.national.com/
Nihon International Electronics Corp.	www.abbsem.com/english/salesb.htm
On Semiconductor	www.onsemi.com
Philips Semiconductors	www.semiconductors.philips.com/catalog/
Power Integrations, Inc.	www.powerint.com/
Powerex, Inc.	www.pwrx.com/
PowerTech, Inc.	www.power-tech.com/
RCA Corp.	www.rca.com/
Rockwell Inc.	www.rockwell.com
Reliance Electric	www.reliance.com
Siemens	www.siemens.com
Silicon Power Corp.	www.siliconpower.com/
Semikron International	www.semikron.com/
Siliconix, Inc.	www.siliconix.com
Tokin, Inc.	www.tokin.com/
Toshiba America Electronic Components, Inc.	www.toshiba.com/taec/
Unitrode Integrated Circuits Corp.	www.unitrode.com/
Westcode Semiconductors Ltd.	www.westcode.com/ws-prod.html

1.11 POWER ELECTRONICS JOURNALS AND CONFERENCES

There are many professional journals and conferences in which the new developments are published. The Institute of Electrical and Electronics Engineers (IEEE) e-library *Explore* is an excellent tool in finding articles published in the IEE journals

and magazines, and in the IEEE journals, magazines, and sponsored conferences. Some of them are:

IEEE e_Library	ieeexplore.ieee.org/
IEEE Transactions on Aerospace and Systems	www.ieee.org/
IEEE Transactions on Industrial Electronics	www.ieee.org/
IEEE Transactions on Industry Applications	www.ieee.org/
IEEE Transactions on Power Delivery	www.ieee.org/
IEEE Transactions on Power Electronics	www.ieee.org/
IEE *Proceedings on Electric Power*	www.iee.org/Publish/

Journal of Electrical Machinery and Power Systems
Applied Power Electronics Conference (APEC)
European Power Electronics Conference (EPEC)
IEEE Industrial Electronics Conference (IECON)
IEEE Industry Applications Society (IAS) Annual Meeting
International Conference on Electrical Machines (ICEM)
International Power Electronics Conference (IPEC)
International Power Electronics Congress (CIEP)
International Telecommunications Energy Conference (INTELEC)
Power Conversion Intelligent Motion (PCIM)
Power Electronics Specialist Conference (PESC)

SUMMARY

As the technology for the power semiconductor devices and integrated circuits develops, the potential for the applications of power electronics becomes wider. There are already many power semiconductor devices that are commercially available; however, the development in this direction is continuing. The power converters fall generally into six categories: (1) rectifiers, (2) ac–dc converters, (3) ac–ac converters, (4) dc–dc converters, (5) dc–ac converters, and (6) static switches. The design of power electronics circuits requires designing the power and control circuits. The voltage and current harmonics that are generated by the power converters can be reduced (or minimized) with a proper choice of the control strategy.

REFERENCES

[1] E. I. Carroll, "Power electronics: where next?" *Power Engineering Journal*, December 1996, pp. 242–243.

[2] S. Bernet, "Recent developments of high power converters for industry and traction applications," *IEEE Transactions on Power Electronics*, Vol. 15, No. 6, November 2000, pp. 1102–1117.

[3] E. I. Carroll, "Power electronics for very high power applications," *Power Engineering Journal*, April 1999, pp. 81–87.

[4] P. K. Steimer, H. E. Gruning, J. Werninger, E. Carroll, S. Klada, and S. Linder, "IGCT—a new emerging for high power, low cost inverters," *IEEE Industry Applications Magazine*, July/August 1999, pp. 12–18.

[5] R. G. Hoft, *Semiconductor Power Electronics*. New York: Van Nostrand Reinhold. 1986.

[6] K. Gadi, "Power electronics in action," *IEEE Spectrum*, July 1995, p. 33.

[7] J. Baliga, "Power ICs in the daddle," *IEEE Spectrum*, July 1995, pp. 34–49.

[8] I. Zverev and J. Hancock, "CoolMOS Selection Guide," Application note: AN-CoolMOS-02, *Infineon Technologies*, June 2000.

[9] "Power Electronics Books," SMPS Technology Knowledge Base, March 1, 1999. www.smpstech.com/books/booklist.htm

[10] "Power Communities," Darnell.Com Inc., March 1, 2002. www.darnell.com/

REVIEW QUESTIONS

1.1 What are power electronics?
1.2 What are the various types of thyristors?
1.3 What is a commutation circuit?
1.4 What are the conditions for a thyristor to conduct?
1.5 How can a conducting thyristor be turned off?
1.6 What is a line commutation?
1.7 What is a forced commutation?
1.8 What is the difference between a thyristor and a TRIAC?
1.9 What is the gating characteristic of a GTO?
1.10 What is the gating characteristic of an MTO?
1.11 What is the gating characteristic of an ETO?
1.12 What is the gating characteristic of an IGCT?
1.13 What is turn-off time of a thyristor?
1.14 What is a converter?
1.15 What is the principle of ac–dc conversion?
1.16 What is the principle of ac–ac conversion?
1.17 What is the principle of dc–dc conversion?
1.18 What is the principle of dc–ac conversion?
1.19 What are the steps involved in designing power electronics equipment?
1.20 What are the peripheral effects of power electronics equipment?
1.21 What are the differences in the gating characteristics of GTOs and thyristors?
1.22 What are the differences in the gating characteristics of thyristors and transistors?
1.23 What are the differences in the gating characteristics of BJTs and MOSFETs?
1.24 What is the gating characteristic of an IGBT?
1.25 What is the gating characteristic of an MCT?
1.26 What is the gating characteristic of an SIT?
1.27 What are the differences between BJTs and IGBTs?
1.28 What are the differences between MCTs and GTOs?
1.29 What are the differences between SITHs and GTOs?

CHAPTER 2

Power Semiconductor Diodes and Circuits

The learning objectives of this chapter are as follows:

- To understand the diode characteristics and its models
- To learn the types of diodes
- To learn the series and parallel operation of diodes
- To learn the SPICE diode model
- To study the effects of a unidirectional device like a diode on *RLC* circuits
- To study the applications of diodes in freewheeling and stored-energy recovery

2.1 INTRODUCTION

Many applications have been found for diodes in electronics and electrical engineering circuits. Power diodes play a significant role in power electronics circuits for conversion of electric power. Some diode circuits that are commonly encountered in power electronics for power processing are reviewed in this chapter.

A diode acts as a switch to perform various functions, such as switches in rectifiers, freewheeling in switching regulators, charge reversal of capacitor and energy transfer between components, voltage isolation, energy feedback from the load to the power source, and trapped energy recovery.

Power diodes can be assumed as ideal switches for most applications but practical diodes differ from the ideal characteristics and have certain limitations. The power diodes are similar to *pn*-junction signal diodes. However, the power diodes have larger power-, voltage-, and current-handling capabilities than those of ordinary signal diodes. The frequency response (or switching speed) is low compared with that of signal diodes.

2.2 SEMICONDUCTOR BASICS

Power semiconductor devices are based on high-purity, single-crystal silicon. Single crystals of several meters long and with the required diameter (up to 150 mm) are

grown in the so-called *float zone* furnaces. Each huge crystal is sliced into thin wafers, which then go through numerous process steps to turn into power devices.

Silicon, is a member of Group IV of the periodic table of elements, that is, having four electrons per atom in its outer orbit. A pure silicon material is known as an *intrinsic semiconductor* with resistivity that is too low to be an insulator and too high to be a conductor. It has high resistivity and very high dielectric strength (over 200 kV/cm). The resistivity of an intrinsic semiconductor and its charge carriers that are available for conduction can be changed, shaped in layers, and *graded* by implantation of specific impurities. The process of adding impurities is called *doping*, which involves a single atom of the added impurity per over a million silicon atoms. With different impurities, levels and shapes of doping, high technology of photolithography, laser cutting, etching, insulation, and packaging, the finished power devices are produced from various structures of n-type and p-type semiconductor layers.

n-Type material: If pure silicon is doped with a small amount of a Group V element, such as phosphorus, arsenic, or antimony, each atom of the *dopant* forms a covalent bond within the silicon lattice, leaving a loose electron. These loose electrons greatly increase the conductivity of the material. When the silicon is lightly doped with an impurity such as phosphorus, the doping is denoted as *n doping* and the resultant material is referred to as *n-type semiconductor.* When it is heavily doped, it is denoted as $n+$ doping and the material is referred to as *n+-type semiconductor.*

p-Type material: If pure silicon is doped with a small amount of a Group III element, such as boron, gallium, or indium, a vacant location called a *hole* is introduced into the silicon lattice. Analogous to an electron, a hole can be considered a mobile charge carrier as it can be filled by an adjacent electron, which in this way leaves a hole behind. These holes greatly increase the conductivity of the material. When the silicon is lightly doped with an impurity such as boron, the doping is denoted as *p-doping* and the resultant material is referred to as *p-type semiconductor.* When it is heavily doped, it is denoted as $p+$ doping and the material is referred to as *p+-type semiconductor.*

Therefore, there are free electrons available in an n-type material and free holes available in a p-type material. In a p-type material the holes are called the majority carriers and electrons are called the minority carriers. In the n-type material, the electrons are called the majority carriers, and holes are called the minority carriers. These carriers are continuously generated by thermal agitations, they combine and recombine in accordance to their lifetime, and they achieve an equilibrium density of carriers from about 10^{10} to $10^{13}/cm^3$ over a range of about 0 °C to 1000 °C. Thus, an applied electric field can cause a current flow in an n-type or p-type material.

Key Points of Section 2.2

- Free electrons or holes are made available by adding impurities to the pure silicon or germanium through a doping process. The electrons are the majority carriers in the n-type material whereas the holes are the majority carriers in a p-type

material. Thus, the application of electric field can cause a current flow in an n-type or a p-type material.

2.3 DIODE CHARACTERISTICS

A power diode is a two-terminal pn-junction device [1, 2] and a pn-junction is normally formed by alloying, diffusion, and epitaxial growth. The modern control techniques in diffusion and epitaxial processes permit the desired device characteristics. Figure 2.1 shows the sectional view of a pn-junction and diode symbol.

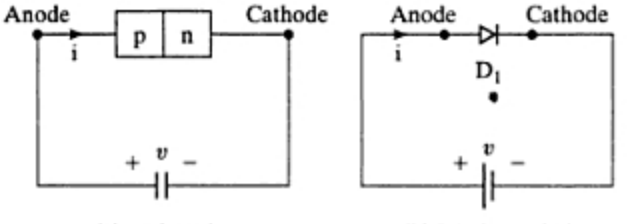
When the anode potential is positive with respect to the cathode, the diode is said to be forward biased and the diode conducts. A conducting diode has a relatively small forward voltage drop across it; and the magnitude of this drop depends on the manufacturing process and junction temperature. When the cathode potential is positive with respect to the anode, the diode is said to be reverse biased. Under reverse-biased conditions, a small reverse current (also known as *leakage current*) in the range of micro- or milliampere, flows and this leakage current increases slowly in magnitude with the reverse voltage until the avalanche or zener voltage is reached. Figure 2.2a shows the steady-state v–i characteristics of a diode. For most practical purposes, a diode can be regarded as an ideal switch, whose characteristics are shown in Figure 2.2b.

The v–i characteristics shown in Figure 2.2a can be expressed by an equation known as *Schockley diode equation*, and it is given under dc steady-state operation by

$$I_D = I_s(e^{V_D/nV_T} - 1) \tag{2.1}$$

where I_D = current through the diode, A;
V_D = diode voltage with anode positive with respect to cathode, V;
I_s = leakage (or reverse saturation) current, typically in the range 10^{-6} to 10^{-15} A;
n = empirical constant known as *emission coefficient*, or *ideality factor*, whose value varies from 1 to 2.

The emission coefficient n depends on the material and the physical construction of the diode. For germanium diodes, n is considered to be 1. For silicon diodes, the predicted value of n is 2, but for most practical silicon diodes, the value of n falls in the range 1.1 to 1.8.



(a) pn-junction (b) Diode symbol

FIGURE 2.1
pn-Junction and diode symbol.

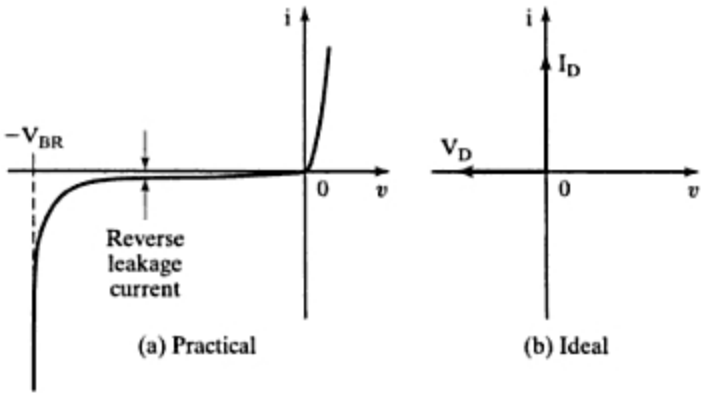


FIGURE 2.2
v–i Characteristics of diode.

(a) Practical (b) Ideal

V_T in Eq. (2.1) is a constant called *thermal voltage* and it is given by

$$V_T = \frac{kT}{q} \tag{2.2}$$

where q = electron charge: 1.6022×10^{-19} coulomb (C);
T = absolute temperature in Kelvin (K = 273 + °C);
k = Boltzmann's constant: 1.3806×10^{-23} J/K.

At a junction temperature of 25 °C, Eq. (2.2) gives

$$V_T = \frac{kT}{q} = \frac{1.3806 \times 10^{-23} \times (273 + 25)}{1.6022 \times 10^{-19}} \approx 25.7 \text{ mV}$$

At a specified temperature, the leakage current I_s is a constant for a given diode. The diode characteristic of Figure 2.2a can be divided into three regions:

Forward-biased region, where $V_D > 0$
Reverse-biased region, where $V_D < 0$
Breakdown region, where $V_D < -V_{BR}$

Forward-biased region. In the forward-biased region, $V_D > 0$. The diode current I_D is very small if the diode voltage V_D is less than a specific value V_{TD} (typically 0.7 V). The diode conducts fully if V_D is higher than this value V_{TD}, which is referred to as the *threshold voltage, cut-in voltage*, or *turn-on voltage*. Thus, the threshold voltage is a voltage at which the diode conducts fully.

Let us consider a small diode voltage $V_D = 0.1$ V, $n = 1$, and $V_T = 25.7$ mV. From Eq. (2.1) we can find the corresponding diode current I_D as

$$I_D = I_s(e^{V_D/nV_T} - 1) = I_s[e^{0.1/(1\times 0.0257)} - 1] = I_s(48.96 - 1) = 47.96\, I_s$$

which can be approximated to $I_D \approx I_s e^{V_D/nV_T} = 48.96\, I_s$, that is, with an error of 2.1%. As v_D increases, the error decreases rapidly.

Therefore, for $V_D > 0.1$ V, which is usually the case, $I_D \gg I_s$, and Eq. (2.1) can be approximated within 2.1% error to

$$I_D = I_s(e^{V_D/nV_T} - 1) \approx I_s e^{V_D/nV_T} \tag{2.3}$$

Reverse-biased region. In the reverse-biased region, $V_D < 0$. If V_D is negative and $|V_D| \gg V_T$, which occurs for $V_D < -0.1$ V, the exponential term in Eq. (2.1) becomes negligibly small compared with unity and the diode current I_D becomes

$$I_D = I_s(e^{-|V_D|/nV_T} - 1) \approx -I_s \tag{2.4}$$

which indicates that the diode current I_D in the reverse direction is constant and equals I_s.

Breakdown region. In the breakdown region, the reverse voltage is high, usually with a magnitude greater than 1000 V. The magnitude of the reverse voltage may exceed a specified voltage known as the *breakdown voltage* V_{BR}, with a small change in reverse voltage beyond V_{BR}. The reverse current increases rapidly. The operation in the breakdown region will not be destructive, provided that the power dissipation is within a "safe level" that is specified in the manufacturer's data sheet. However, it is often necessary to limit the reverse current in the breakdown region to limit the power dissipation within a permissible value.

Example 2.1 Finding the Saturation Current

The forward voltage drop of a power diode is $V_D = 1.2$ V at $I_D = 300$ A. Assuming that $n = 2$ and $V_T = 25.7$ mV, find the reverse saturation current I_s.

Solution

Applying Eq. (2.1), we can find the leakage (or saturation) current I_s from

$$300 = I_s[e^{1.2/(2\times 25.7\times 10^{-3})} - 1]$$

which gives $I_s = 2.17746 \times 10^{-8}$ A.

Key Points of Section 2.3

- A diode exhibits a nonlinear v–i characteristic, consisting of three regions: forward biased, reverse-biased, and breakdown. In the forward condition the diode drop is small, typically 0.7 V. If the reverse voltage exceeds the breakdown voltage, the diode may be damaged.

2.4 REVERSE RECOVERY CHARACTERISTICS

The current in a forward-biased junction diode is due to the net effect of majority and minority carriers. Once a diode is in a forward conduction mode and then its forward current is reduced to zero (due to the natural behavior of the diode circuit or application of a reverse voltage), the diode continues to conduct due to minority carriers that remain stored in the *pn*-junction and the bulk semiconductor material. The minority carriers require a certain time to recombine with opposite charges and to be neutralized. This time

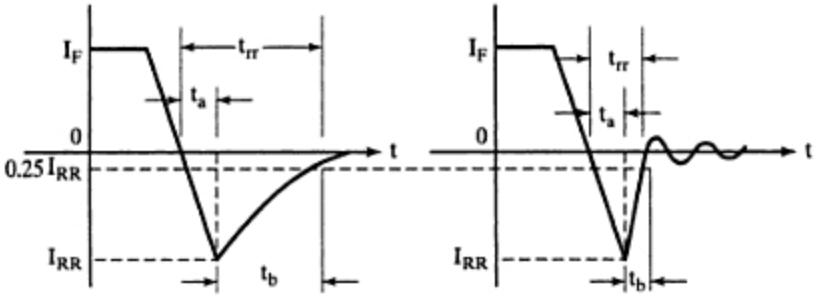


FIGURE 2.3

Reverse recovery characteristics.

is called the *reverse recovery time* of the diode. Figure 2.3 shows two reverse recovery characteristics of junction diodes. The soft-recovery type is more common. The reverse recovery time is denoted as t_{rr} and is measured from the initial zero crossing of the diode current to 25% of maximum (or peak) reverse current I_{RR}. The t_{rr} consists of two components, t_a and t_b. Variable t_a is due to charge storage in the depletion region of the junction and represents the time between the zero crossing and the peak reverse current I_{RR}. The t_b is due to charge storage in the bulk semiconductor material. The ratio t_b/t_a is known as the *softness factor* (SF). For practical purposes, one needs be concerned with the total recovery time t_{rr} and the peak value of the reverse current I_{RR}.

$$t_{rr} = t_a + t_b \tag{2.5}$$

The peak reverse current can be expressed in reverse di/dt as

$$I_{RR} = t_a \frac{di}{dt} \tag{2.6}$$

Reverse recovery time t_{rr}, may be defined as the time interval between the instant the current passes through zero during the changeover from forward conduction to reverse blocking condition and the moment the reverse current has decayed to 25% of its peak reverse value I_{RR}. Variable t_{rr} is dependent on the junction temperature, rate of fall of forward current, and forward current prior to commutation, I_F.

Reverse recovery charge Q_{RR}, is the amount of charge carriers that flows across the diode in the reverse direction due to changeover from forward conduction to reverse blocking condition. Its value is determined from the area enclosed by the path of the reverse recovery current.

The storage charge, which is the area enclosed by the path of the recovery current, is approximately

$$Q_{RR} \cong \tfrac{1}{2} I_{RR} t_a + \tfrac{1}{2} I_{RR} t_b = \tfrac{1}{2} I_{RR} t_{rr} \tag{2.7}$$

or

$$I_{RR} \cong \frac{2Q_{RR}}{t_{rr}} \tag{2.8}$$

Equating I_{RR} in Eq. (2.6) to I_{RR} in Eq. (2.8) gives

$$t_{rr}t_a = \frac{2Q_{RR}}{di/dt} \tag{2.9}$$

If t_b is negligible as compared to t_a, which is usually the case, $t_{rr} \approx t_a$, and Eq. (2.9) becomes

$$t_{rr} \cong \sqrt{\frac{2Q_{RR}}{di/dt}} \tag{2.10}$$

and

$$I_{RR} = \sqrt{2Q_{RR}\frac{di}{dt}} \tag{2.11}$$

It can be noticed from Eqs. (2.10) and (2.11) that the reverse recovery time t_{rr} and the peak reverse recovery current I_{RR} depend on the storage charge Q_{RR} and the reverse (or reapplied) di/dt. The storage charge is dependent on the forward diode current I_F. The peak reverse recovery current I_{RR}, reverse charge Q_{RR}, and the SF are all of interest to the circuit designer, and these parameters are commonly included in the specification sheets of diodes.

If a diode is in a reverse-biased condition, a leakage current flows due to the minority carriers. Then the application of forward voltage would force the diode to carry current in the forward direction. However, it requires a certain time known as *forward recovery (or turn-on) time* before all the majority carriers over the whole junction can contribute to the current flow. If the rate of rise of the forward current is high and the forward current is concentrated to a small area of the junction, the diode may fail. Thus, the forward recovery time limits the rate of the rise of the forward current and the switching speed.

Example 2.2 Finding the Reverse Recovery Current

The reverse recovery time of a diode is $t_{rr} = 3\ \mu s$ and the rate of fall of the diode current is $di/dt = 30\ A/\mu s$. Determine (a) the storage charge Q_{RR}, and (b) the peak reverse current I_{RR}.

Solution

$t_{rr} = 3\ \mu s$ and $di/dt = 30\ A/\mu s$.

a. From Eq. (12.10),

$$Q_{RR} = \tfrac{1}{2}\frac{di}{dt}t_{rr}^2 = 0.5 \times 30\ A/\mu s \times (3 \times 10^{-6})^2 = 135\ \mu C$$

b. From Eq. (2.11),

$$I_{RR} = \sqrt{2Q_{RR}\frac{di}{dt}} = \sqrt{2 \times 135 \times 10^{-6} \times 30 \times 10^{6}} = 90\ A$$

Key Points of Section 2.4

- During the reverse recovery time t_{rr}, the diode behaves effectively as a short circuit and is not capable of blocking reverse voltage, allowing reverse current flow, and then suddenly disrupting the current. Parameter t_{rr} is important for switching applications.

2.5 POWER DIODE TYPES

Ideally, a diode should have no reverse recovery time. However, the manufacturing cost of such a diode may increase. In many applications, the effects of reverse recovery time is not significant, and inexpensive diodes can be used. Depending on the recovery characteristics and manufacturing techniques, the power diodes can be classified into the following three categories:

1. Standard or general-purpose diodes
2. Fast-recovery diodes
3. Schottky diodes

The characteristics and practical limitations of these types restrict their applications.

2.5.1 General-Purpose Diodes

The general-purpose rectifier diodes have relatively high reverse recovery time, typically 25 μs; and are used in low-speed applications, where recovery time is not critical (e.g., diode rectifiers and converters for a low-input frequency up to 1-kHz applications and line-commutated converters). These diodes cover current ratings from less than 1 A to several thousands of amperes, with voltage ratings from 50 V to around 5 kV. These diodes are generally manufactured by diffusion. However, alloyed types of rectifiers that are used in welding power supplies are most cost-effective and rugged, and their ratings can go up to 1500 V, 400 A.

Figure 2.4 shows various configurations of general-purpose diodes, which basically fall into two types. One is called a *stud*, or *stud-mounted* type; the other one is called a *disk*, *press pak*, or *hockey-puck* type. In a stud-mounted type, either the anode or the cathode could be the stud.

2.5.2 Fast-Recovery Diodes

The fast-recovery diodes have low recovery time, normally less than 5 μs. They are used in dc–dc and dc–ac converter circuits, where the speed of recovery is often of critical importance. These diodes cover current ratings of voltage from 50 V to around 3 kV, and from less than 1 A to hundreds of amperes.

For voltage ratings above 400 V, fast-recovery diodes are generally made by diffusion and the recovery time is controlled by platinum or gold diffusion. For voltage ratings below 400 V, epitaxial diodes provide faster switching speeds than those of diffused diodes. The epitaxial diodes have a narrow base width, resulting in a fast recovery time of as low as 50 ns. Fast-recovery diodes of various sizes are shown in Figure 2.4.

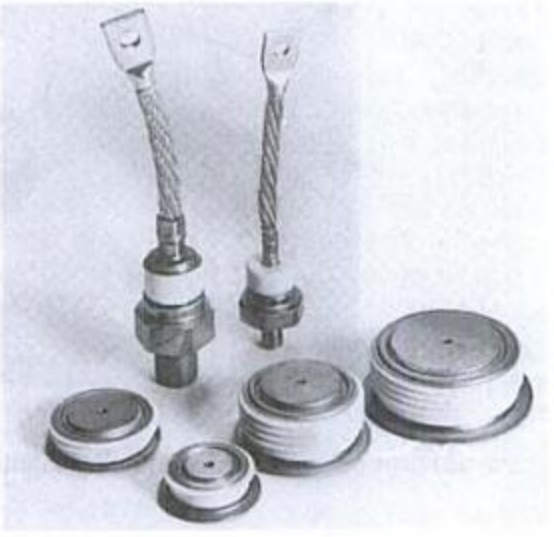


FIGURE 2.4
Fast-recovery diodes. (Courtesy of Powerex, Inc.)

2.5.3 Schottky Diodes

The charge storage problem of a *pn*-junction can be eliminated (or minimized) in a Schottky diode. It is accomplished by setting up a "barrier potential" with a contact between a metal and a semiconductor. A layer of metal is deposited on a thin epitaxial layer of *n*-type silicon. The potential barrier simulates the behavior of a *pn*-junction. The rectifying action depends on the majority carriers only, and as a result there are no excess minority carriers to recombine. The recovery effect is due solely to the self-capacitance of the semiconductor junction.

The recovered charge of a Schottky diode is much less than that of an equivalent *pn*-junction diode. Because it is due only to the junction capacitance, it is largely independent of the reverse *di/dt*. A Schottky diode has a relatively low forward voltage drop.

The leakage current of a Schottky diode is higher than that of a *pn*-junction diode. A Schottky diode with relatively low-conduction voltage has relatively high leakage current, and vice versa. As a result, the maximum allowable voltage of this diode is generally limited to 100 V. The current ratings of Schottky diodes vary from 1 to 400 A. The Schottky diodes are ideal for high-current and low-voltage dc power supplies. However, these diodes are also used in low-current power supplies for increased efficiency. In Figure 2.5, 20- and 30-A dual Schottky rectifiers are shown.

Key Points of Section 2.5

- Depending on the switching recovery time and the on-state drop, the power diodes are of three types: general purpose, fast recovery, and Schottky.

2.6 SILICON CARBIDE DIODES

Silicon Carbide (SiC) is a new material for power electronics. Its physical properties outperform Si and GaAs by far. For example, the Schottky SiC diodes manufactured

FIGURE 2.5
Dual Schottky center rectifiers of 20 and 30 A. (Courtesy of International Rectifier.)

by Infineon Technologies [3] have ultralow power losses and high reliability. They also have the following features:

- No reverse recovery time;
- Ultrafast switching behavior;
- No temperature influence on the switching behavior.

The typical storage charge Q_{RR} is 21 nC for a 600-V, 6-A diode and is 23 nC for a 600-V, 10-A, device.

2.7 SPICE DIODE MODEL

The SPICE model of a diode [4–6] is shown in Figure 2.6a. The diode current I_D that depends on its voltage is represented by a current source. R_s is the series resistance, and it is due to the resistance of the semiconductor. R_s, also known as *bulk resistance*, is dependent on the amount of doping. The small-signal and static models that are generated by SPICE are shown in Figures 2.6b and 12.6c, respectively. C_D is a nonlinear function of the diode voltage v_D and is equal to $C_D = dq_d/dv_D$, where q_d is the depletion-layer charge. SPICE generates the small-signal parameters from the operating point.

The SPICE model statement of a diode has the general form

```
.MODEL DNAME D (P1=V1 P2=V2 P3=V3 ..... PN=VN)
```

DNAME is the model name and it can begin with any character; however, its word size is normally limited to 8. D is the type symbol for diodes. P1, P2, ... and V1, V2, ... are the model parameters and their values, respectively.

Among many diode parameters, the important parameters [5] for power switching are:

IS	Saturation current
BV	Reverse breakdown voltage
IBV	Reverse breakdown current
TT	Transit time
CJO	Zero-bias *pn* capacitance

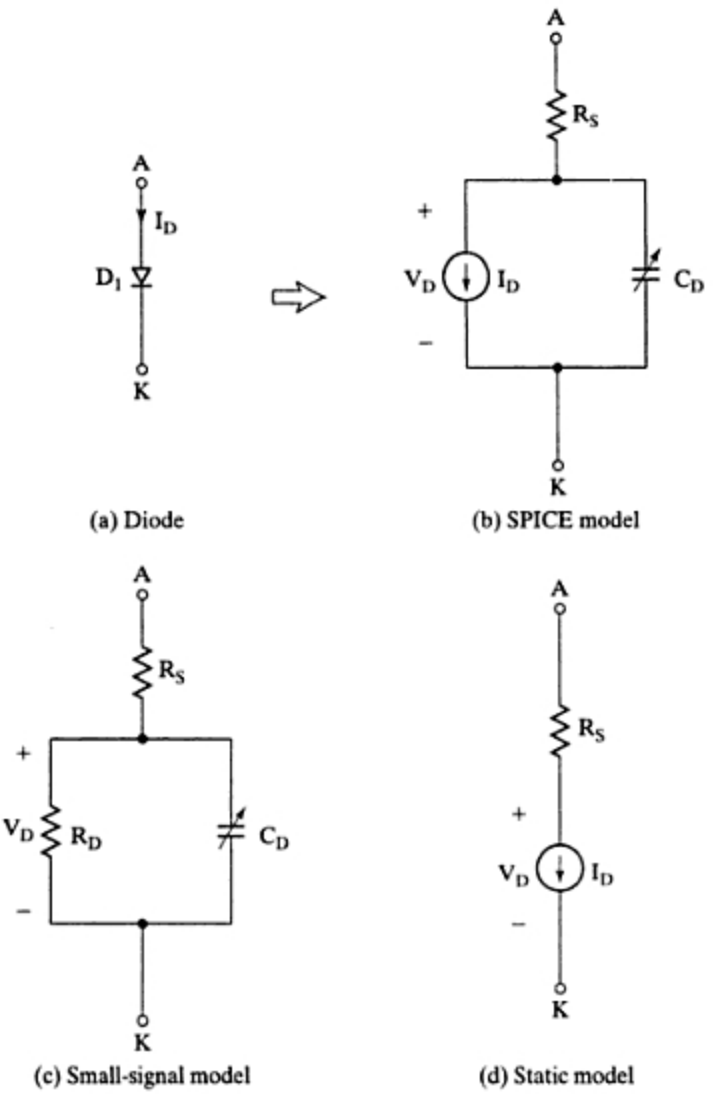


FIGURE 2.6

SPICE diode model with reverse-biased diode.

Because the SiC diodes use a completely new type of technology, the use of SPICE models for silicon diodes may introduce a significant amount of errors. The manufacturers [3] are, however, providing the SPICE models of SiC diodes.

Key Points of Section 2.7

- The SPICE parameters, which can be derived from the data sheet, may significantly affect the transient behavior of a switching circuit.

2.8 SERIES-CONNECTED DIODES

In many high-voltage applications (e.g., high-voltage direct current [HVDC] transmission lines), one commercially available diode cannot meet the required voltage rating, and diodes are connected in series to increase the reverse blocking capabilities.

.Let us consider two series-connected diodes as shown in Figure 2.7a. Variables i_D and v_D are the current and voltage, respectively, in the forward direction; v_{D1} and v_{D2} are the sharing reverse voltages of diodes D_1 and D_2, respectively. In practice, the v–i characteristics for the same type of diodes differ due to tolerances in their production process. Figure 2.7b shows two v–i characteristics for such diodes. In the forward-biased condition, both diodes conduct the same amount of current, and the forward voltage drop of each diode would be almost equal. However, in the reverse blocking condition, each diode has to carry the same leakage current, and as a result the blocking voltages may differ significantly.

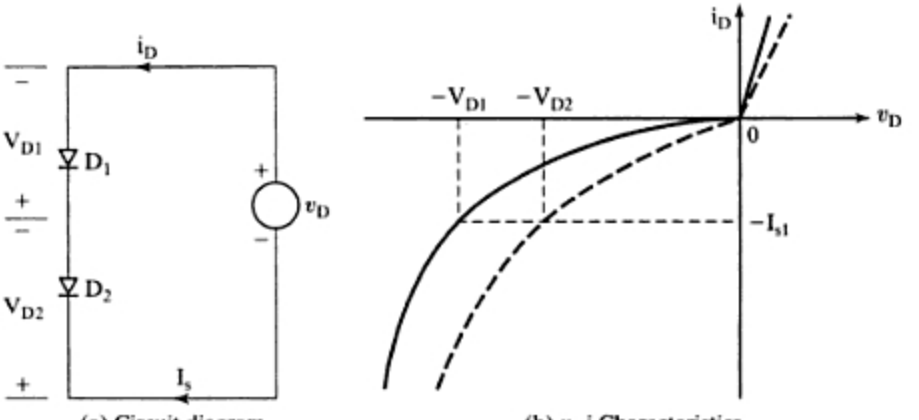
A simple solution to this problem, as shown in Figure 2.8a, is to force equal voltage sharing by connecting a resistor across each diode. Due to equal voltage sharing, the leakage current of each diode would be different, and this is shown in Figure 2.8b. Because the total leakage current must be shared by a diode and its resistor,

$$I_s = I_{s1} + I_{R1} = I_{s2} + I_{R2} \tag{2.12}$$

However, $I_{R1} = V_{D1}/R_1$ and $I_{R2} = V_{D2}/R_2 = V_{D1}/R_2$. Equation (2.12) gives the relationship between R_1 and R_2 for equal voltage sharing as

$$I_{s1} + \frac{V_{D1}}{R_1} = I_{s2} + \frac{V_{D1}}{R_2} \tag{2.13}$$

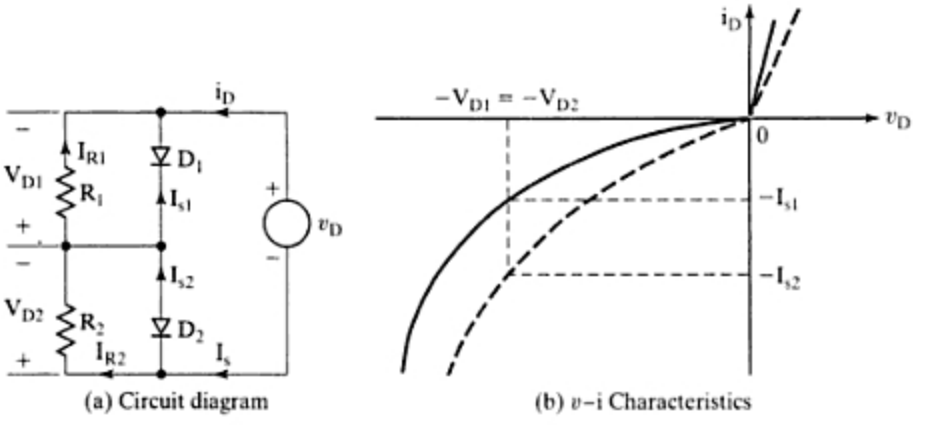
If the resistances are equal, then $R = R_1 = R_2$ and the two diode voltages would be slightly different depending on the dissimilarities of the two v–i characteristics. The



(a) Circuit diagram (b) v–i Characteristics

FIGURE 2.7

Two series-connected diodes with reverse bias.



(a) Circuit diagram (b) v–i Characteristics

FIGURE 2.8

Series-connected diodes with steady-state voltage-sharing characteristics.

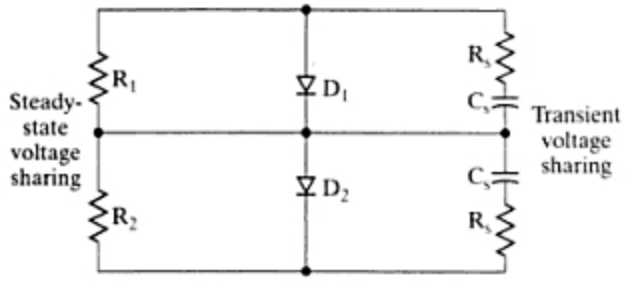


FIGURE 2.9

Series diodes with voltage-sharing networks under steady-state and transient conditions.

values of V_{D1} and V_{D2} can be determined from Eqs. (2.14) and (2.15):

$$I_{s1} + \frac{V_{D1}}{R} = I_{s2} + \frac{V_{D2}}{R} \tag{2.14}$$

$$V_{D1} + V_{D2} = V_s \tag{2.15}$$

The voltage sharings under transient conditions (e.g., due to switching loads, the initial applications of the input voltage) are accomplished by connecting capacitors across each diode, which is shown in Figure 2.9. R_s limits the rate of rise of the blocking voltage.

Example 2.3 Finding the Voltage Sharing Resistors

Two diodes are connected in series, shown in Figure 2.8a to share a total dc reverse voltage of $V_D = 5$ kV. The reverse leakage currents of the two diodes are $I_{s1} = 30$ mA and $I_{s2} = 35$ mA. (a) Find the diode voltages if the voltage-sharing resistances are equal, $R_1 = R_2 = R = 100\,\text{k}\Omega$. (b) Find the voltage-sharing resistances R_1 and R_2 if the diode voltages are equal, $V_{D1} = V_{D2} = V_D/2$. (c) Use PSpice to check your results of part (a). PSpice model parameters of the diodes are BV = 3 kV and IS = 30 mA for diode D_1, and IS = 35 mA for diode D_2.

Solution

a. $I_{s1} = 30\,\text{mA}$, $I_{s2} = 35\,\text{mA}$, and $R_1 = R_2 = R = 100\,\text{k}\Omega$. $-V_D = -V_{D1} - V_{D2}$ or $V_{D2} = V_D - V_{D1}$. From Eq. (2.14),

$$I_{s1} + \frac{V_{D1}}{R} = I_{s2} + \frac{V_{D2}}{R}$$

Substituting $V_{D2} = V_D - V_{D1}$ and solving for the diode voltage D_1, we get

$$V_{D1} = \frac{V_D}{2} + \frac{R}{2}(I_{s2} - I_{s1})$$

$$= \frac{5\,\text{kV}}{2} + \frac{100\,\text{k}\Omega}{2}(35 \times 10^{-3} - 30 \times 10^{-3}) = 2750\,\text{V} \tag{2.16}$$

and $V_{D2} = V_D - V_{D1} = 5\,\text{kV} - 2750 = 2250\,\text{V}$.

b. $I_{s1} = 30\,\text{mA}$, $I_{s2} = 35\,\text{mA}$, and $V_{D1} = V_{D2} = V_D/2 = 2.5\,\text{kV}$. From Eq. (2.13),

$$I_{s1} + \frac{V_{D1}}{R_1} = I_{s2} + \frac{V_{D2}}{R_2}$$

which gives the resistance R_2 for a known value of R_1 as

$$R_2 = \frac{V_{D2}R_1}{V_{D1} - R_1(I_{s2} - I_{s1})} \tag{2.17}$$

Assuming that $R_1 = 100\,\text{k}\Omega$, we get

$$R_2 = \frac{2.5\,\text{kV} \times 100\,\text{k}\Omega}{2.5\,\text{kV} - 100\,\text{k}\Omega \times (35 \times 10^{-3} - 30 \times 10^{-3})} = 125\,\text{k}\Omega$$

c. The diode circuit for PSpice simulation is shown in Figure 2.10. The list of the circuit file is as follows:

```
Example 2.3          Diode Voltage-Sharing Circuit
VS      1      0     DC      5KV
R       1      2     0.01
R1      2      3     100K
R2      3      0     100K
D1      3      2     MOD1
D2      0      3     MOD2
.MODEL MOD1 D (IS=30MA BV=3KV)     ; Diode model parameters
.MODEL MOD2 D (IS=35MA BV=3KV)     ; Diode model parameters
.OP                                ; Dc operating point analysis
.END
```

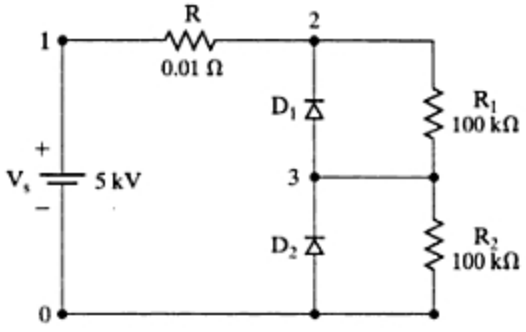


FIGURE 2.10
Diode circuit for PSpice simulation for Example 2.3.

The results of PSpice simulation are

NAME	D1	D2
ID	-3.00E-02 I_{D1}=-30 mA	-3.50E-02 I_{D2}=-35 mA
VD	-2.75E+03 V_{D1}=-2750 V expected -2750 V	-2.25E+03 V_{D2}=-2250 V expected -2250 V
REQ	1.00E+12 R_{D1}=1 GΩ	1.00E+12 R_{D2}=1 GΩ

Note: The SPICE gives the same voltages as expected. A small resistance of $R = 10\ \text{m}\Omega$ is inserted to avoid SPICE error due to a zero-resistance voltage loop.

Key Points of Section 2.8

- When diodes of the same type are connected in series, they do not share the same reverse voltage due to mismatches in their reverse $v-i$ characteristics. Voltage-sharing networks are needed to equalize the voltage sharing.

2.9 PARALLEL-CONNECTED DIODES

In high-power applications, diodes are connected in parallel to increase the current-carrying capability to meet the desired current requirements. The current sharings of diodes would be in accord with their respective forward voltage drops. Uniform current sharing can be achieved by providing equal inductances (e.g., in the leads) or by connecting current-sharing resistors (which may not be practical due to power losses); and this is depicted in Figure 2.11. It is possible to minimize this problem by selecting diodes with equal forward voltage drops or diodes of the same type. Because the diodes are connected in parallel, the reverse blocking voltages of each diode would be the same.

The resistors of Figure 2.11a help current sharing under steady-state conditions. Current sharing under dynamic conditions can be accomplished by connecting coupled inductors as shown in Figure 2.11b. If the current through D_1 rises, the $L\,di/dt$ across L_1 increases, and a corresponding voltage of opposite polarity is induced across inductor L_2. The result is a low-impedance path through diode D_2 and the current is shifted to D_2. The inductors may generate voltage spikes and they may be expensive and bulky, especially at high currents.

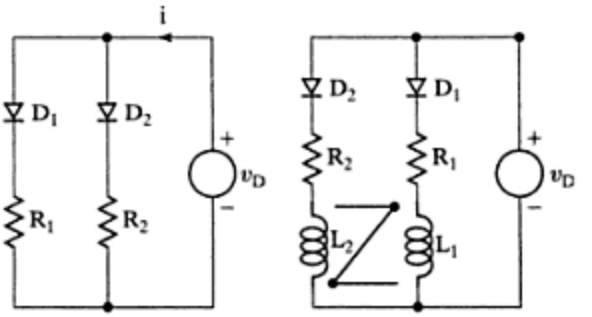


FIGURE 2.11
Parallel-connected diodes.

(a) Steady-state (b) Dynamic sharing

Key Points of Section 2.9

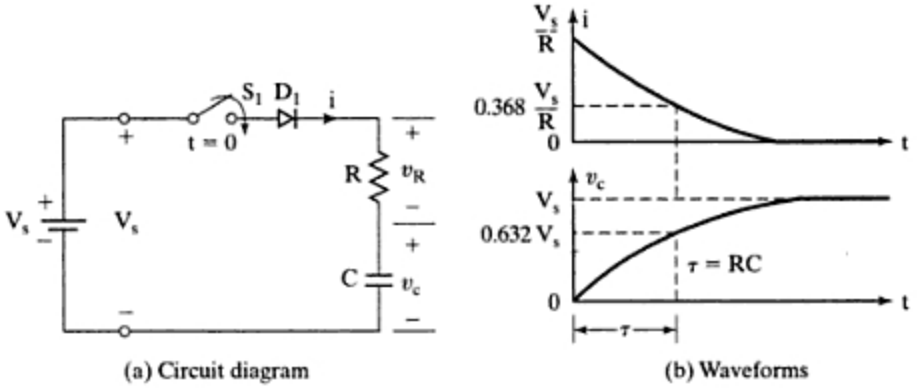
- When diodes of the same type are connected in parallel, they do not share the same on-state current due to mismatches in their forward v–i characteristics. Current sharing networks are needed to equalize the current sharing.

2.10 DIODES WITH *RC* AND *RL* LOADS

Figure 2.12a shows a diode circuit with an *RC* load. For the sake of simplicity the diodes are considered to be ideal. By "ideal" we mean that the reverse recovery time t_{rr} and the forward voltage drop V_D are negligible. That is, $t_{rr} = 0$ and $V_D = 0$. The source voltage V_S is a dc constant voltage. When the switch S_1 is closed at $t = 0$, the charging current i that flows through the capacitor can be found from

$$V_s = v_R + v_c = v_R + \frac{1}{C}\int_{t_0}^{t} i\,dt + v_c(t = 0) \tag{2.18}$$

$$v_R = Ri \tag{2.19}$$



(a) Circuit diagram (b) Waveforms

FIGURE 2.12
Diode circuit with an *RC* load.

With initial condition $v_c(t = 0) = 0$, the solution of Eq. (2.18) (which is derived in Appendix D, Eq. D.1) gives the charging current i as

$$i(t) = \frac{V_s}{R} e^{-t/RC} \tag{2.20}$$

The capacitor voltage v_c is

$$v_c(t) = \frac{1}{C}\int_0^t i\,dt = V_s(1 - e^{-t/RC}) = V_s(1 - e^{-t/\tau}) \tag{2.21}$$

where $\tau = RC$ is the time constant of an RC load. The rate of change of the capacitor voltage is

$$\frac{dv_c}{dt} = \frac{V_s}{RC} e^{-t/RC} \tag{2.22}$$

and the initial rate of change of the capacitor voltage (at $t = 0$) is obtained from Eq. (2.22)

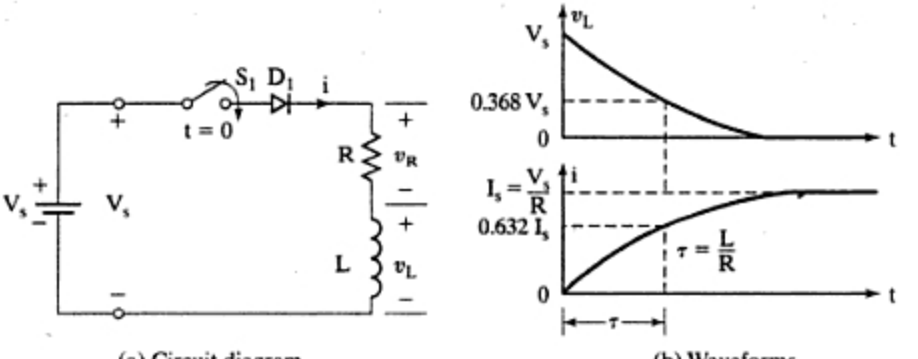
$$\left.\frac{dv_c}{dt}\right|_{t=0} = \frac{V_s}{RC} \tag{2.23}$$

A diode circuit with an RL load is shown in Figure 2.13a. When switch S_1 is closed at $t = 0$, the current i through the inductor increases and is expressed as

$$V_s = v_L + v_R = L\frac{di}{dt} + Ri \tag{2.24}$$

With initial condition $i(t = 0) = 0$, the solution of Eq. (2.24) (which is derived in Appendix D, Eq. D.2) yields

$$i(t) = \frac{V_s}{R}(1 - e^{-tR/L}) \tag{2.25}$$



(a) Circuit diagram (b) Waveforms

FIGURE 2.13
Diode circuit with an RL load.

The rate of change of this current can be obtained from Eq. (2.25) as

$$\frac{di}{dt} = \frac{V_s}{L} e^{-tR/L} \tag{2.26}$$

and the initial rate of rise of the current (at $t = 0$) is obtained from Eq. (2.26):

$$\left.\frac{di}{dt}\right|_{t=0} = \frac{V_s}{L} \tag{2.27}$$

The voltage v_L across the inductor is

$$v_L(t) = L\frac{di}{dt} = V_s e^{-tR/L} \tag{2.28}$$

where $L/R = \tau$ is the time constant of an RL load.

The waveforms for voltage v_L and current are shown in Figure 2.13b. If $t \gg L/R$, the voltage across the inductor tends to be zero and its current reaches a steady-state value of $I_s = V_s/R$. If an attempt is then made to open switch S_1, the energy stored in the inductor ($= 0.5Li^2$) will be transformed into a high reverse voltage across the switch and diode. This energy dissipates in the form of sparks across the switch; and diode D_1 is likely to be damaged in this process. To overcome such a situation, a diode commonly known as a *freewheeling diode* is connected across an inductive load as shown in Figure 2.21a.

Note: Because the current i in Figures 2.12a and 2.13a is unidirectional and does not tend to change its polarity, the diodes have no effect on circuit operation.

Key Points of Section 2.10

- The current of an RC or RL circuit that rises or falls exponentially with a circuit time constant does not reverse its polarity. The initial dv/dt of a charging capacitor in an RC circuit is V_s/RC, and the initial di/dt in an RL circuit is V_s/L.

Example 2.4 Finding the Peak Current and Energy Loss in an RC Circuit

A diode circuit is shown in Figure 2.14a with $R = 44\ \Omega$ and $C = 0.1\ \mu F$. The capacitor has an initial voltage, $V_{c0} = V_c(t = 0) = 220$ V. If switch S_1 is closed at $t = 0$, determine (a) the peak diode current, (b) the energy dissipated in the resistor R, and (c) the capacitor voltage at $t = 2\ \mu s$.

Solution

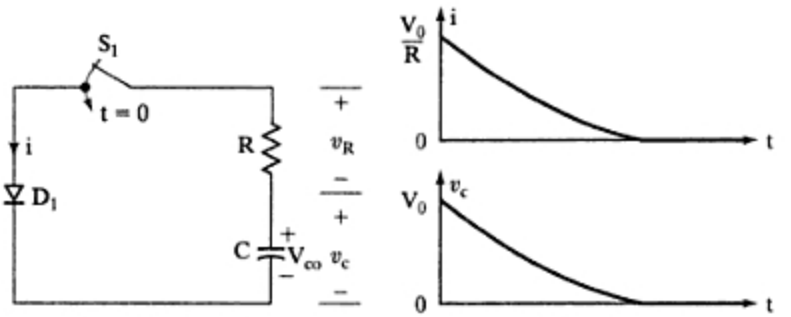
The waveforms are shown in Figure 2.14b.

a. Equation (2.20) can be used with $V_s = V_{c0}$ and the peak diode current I_p is

$$I_p = \frac{V_{c0}}{R} = \frac{220}{44} = 5\ \text{A}$$

b. The energy W dissipated is

$$W = 0.5CV_{c0}^2 = 0.5 \times 0.1 \times 10^{-6} \times 220^2 = 0.00242\ \text{J} = 2.42\ \text{mJ}$$



(a) Circuit diagram (b) Waveforms

FIGURE 2.14
Diode circuit with an *RC* load.

c. For $RC = 44 \times 0.1\ \mu = 4.4\ \mu s$ and $t = t_1 = 2\ \mu s$, the capacitor voltage is

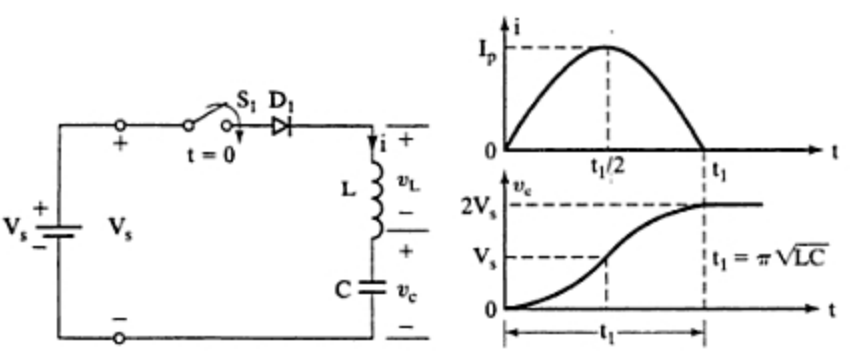
$$v_c(t = 2\ \mu s) = V_{c0}e^{-t/RC} = 220 \times e^{-2/4.4} = 139.64\ V$$

Note: Because the current is unidirectional, the diode does not affect circuit operation.

2.11 DIODES WITH *LC* AND *RLC* LOADS

A diode circuit with an *LC* load is shown in Figure 2.15a. The source voltage V_s is a dc constant voltage. When switch S_1 is closed at $t = 0$, the charging current i of the capacitor is expressed as

$$V_s = L\frac{di}{dt} + \frac{1}{C}\int_{t_0}^{t} i\,dt + v_c(t = 0) \tag{2.29}$$



(a) Circuit diagrams (b) Waveforms

FIGURE 2.15
Diode circuit with an *LC* load.

With initial conditions $i(t = 0) = 0$ and $v_c(t = 0) = 0$, Eq. (2.29) can be solved for the capacitor current i as (in Appendix D, Eq. D.3)

$$i(t) = V_s\sqrt{\frac{C}{L}}\sin \omega_0 t \tag{2.30}$$

$$= I_p \sin \omega_0 t \tag{2.31}$$

where $\omega_0 = 1/\sqrt{LC}$ and the peak current I_p is

$$I_p = V_s\sqrt{\frac{C}{L}} \tag{2.32}$$

The rate of rise of the current is obtained from Eq. (2.30) as

$$\frac{di}{dt} = \frac{V_s}{L}\cos \omega_0 t \tag{2.33}$$

and Eq. (2.33) gives the initial rate of rise of the current (at $t = 0$) as

$$\left.\frac{di}{dt}\right|_{t=0} = \frac{V_s}{L} \tag{2.34}$$

The voltage v_c across the capacitor can be derived as

$$v_c(t) = \frac{1}{C}\int_0^t i\, dt = V_s(1 - \cos \omega_0 t) \tag{2.35}$$

At a time $t = t_1 = \pi\sqrt{LC}$, the diode current i falls to zero and the capacitor is charged to $2V_s$. The waveforms for the voltage v_L and current i are shown in Figure 2.15b.

Note: Because there is no resistance in the circuit, there can be no energy loss. Thus, in the absence of any resistance, the current of an LC circuit oscillates and the energy is transferred from C to L and vice versa.

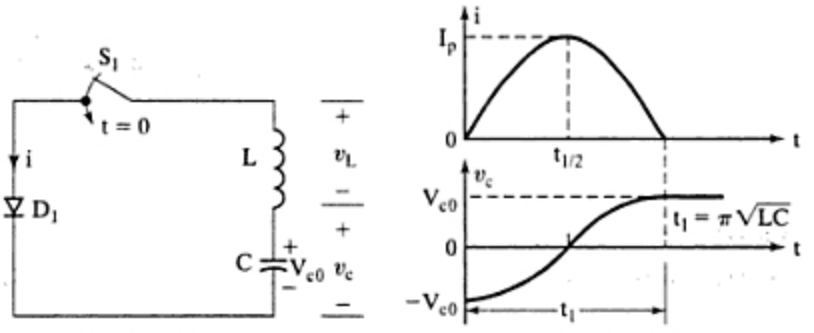
Example 2.5 Finding the Voltage and Current in an *LC* Circuit

A diode circuit with an LC load is shown in Figure 2.16a with the capacitor having an initial voltage; $V_c(t = 0) = -V_{c0} = V_0 - 220$ V, capacitance, $C = 20$ μF; and inductance, $L = 80$ μH. If switch S_1 is closed at $t = 0$, determine (a) the peak current through the diode, (b) the conduction time of the diode, and (c) the final steady-state capacitor voltage.

Solution

a. Using *Kirchhoff's voltage law* (KVL), we can write the equation for the current i as

$$L\frac{di}{dt} + \frac{1}{C}\int_{t_0}^{t} i\, dt + v_c(t = 0) = 0$$



(a) Circuit diagram (b) Waveforms

FIGURE 2.16
Diode circuit with an *LC* load.

and the current i with initial conditions of $i(t = 0) = 0$ and $v_c(t = 0) = -V_{c0}$ is solved as

$$i(t) = V_{c0}\sqrt{\frac{C}{L}}\sin \omega_0 t$$

where $\omega_0 = 1/\sqrt{LC} = 10^6/\sqrt{20 \times 80} = 25{,}000$ rad/s. The peak current I_p is

$$I_p = V_{c0}\sqrt{\frac{C}{L}} = 220\sqrt{\frac{20}{80}} = 110 \text{ A}$$

b. At $t = t_1 = \pi\sqrt{LC}$, the diode current becomes zero and the conduction time t_1 of diode is

$$t_1 = \pi\sqrt{LC} = \pi\sqrt{20 \times 80} = 125.66 \text{ μs}$$

c. The capacitor voltage can easily be shown to be

$$v_c(t) = \frac{1}{C}\int_0^t i\,dt - V_{c0} = -V_{c0}\cos \omega_0 t$$

For $t = t_1 = 125.66$ μs, $v_c(t = t_1) = -220 \cos \pi = 220$ V.

A diode circuit with an *RLC* load is shown in Figure 2.17. If switch S_1 is closed at $t = 0$, we can use the KVL to write the equation for the load current i as

$$L\frac{di}{dt} + Ri + \frac{1}{C}\int i\,dt + v_c(t = 0) = V_s \tag{2.36}$$

with initial conditions $i(t = 0)$ and $v_c(t = 0) = V_{c0}$. Differentiating Eq. (2.36) and dividing both sides by L gives the characteristic equation

$$\frac{d^2i}{dt^2} + \frac{R}{L}\frac{di}{dt} + \frac{i}{LC} = 0 \tag{2.37}$$

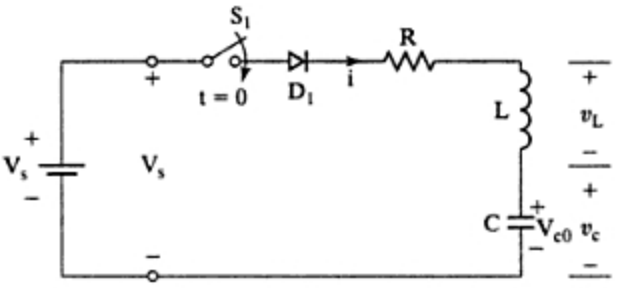


FIGURE 2.17
Diode circuit with an *RLC* load.

Under final steady-state conditions, the capacitor is charged to the source voltage V_s and the steady-state current is zero. The forced component of the current in Eq. (2.37) is also zero. The current is due to the natural component.

The characteristic equation in Laplace's domain of s is

$$s^2 + \frac{R}{L}s + \frac{1}{LC} = 0 \tag{2.38}$$

and the roots of quadratic equation (2.38) are given by

$$s_{1,2} = -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}} \tag{2.39}$$

Let us define two important properties of a second-order circuit: the *damping factor*,

$$\alpha = \frac{R}{2L} \tag{2.40}$$

and the *resonant frequency*,

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2.41}$$

Substituting these into Eq. (2.39) yields

$$s_{1,2} = -\alpha \pm \sqrt{\alpha^2 - \omega_0^2} \tag{2.42}$$

The solution for the current, which depends on the values of α and ω_0, would follow one of the three possible cases.

Case 1. If $\alpha = \omega_0$, the roots are equal, $s_1 = s_2$, and the circuit is called *critically damped*. The solution takes the form

$$i(t) = (A_1 + A_2 t)e^{s_1 t} \tag{2.43}$$

Case 2. If $\alpha > \omega_0$, the roots are real and the circuit is said to be *over-damped*. The solution takes the form

$$i(t) = A_1 e^{s_1 t} + A_2 e^{s_2 t} \tag{2.44}$$

Case 3. If $\alpha < \omega_0$, the roots are complex and the circuit is said to be *underdamped*. The roots are

$$s_{1,2} = -\alpha \pm j\omega_r \tag{2.45}$$

where ω_r is called the *ringing frequency* (or damped resonant frequency) and $\omega_r = \sqrt{\omega_0^2 - \alpha^2}$. The solution takes the form

$$i(t) = e^{-\alpha t}(A_1 \cos \omega_r t + A_2 \sin \omega_r t) \tag{2.46}$$

which is a *damped* or *decaying sinusoidal.*

Note: The constants A_1 and A_2 can be determined from the initial conditions of the circuit. The ratio of α/ω_0 is commonly known as the *damping ratio*, $\delta = R/2\sqrt{C/L}$. Power electronic circuits are generally underdamped such that the circuit current becomes near sinusoidal, to cause a nearly sinusoidal ac output or to turn off a power semiconductor device.

Example 2.6 Finding the Current in an *RLC* Circuit

The second-order *RLC* circuit of Figure 2.17 has the dc source voltage $V_s = 220$ V, inductance $L = 2$ mH, capacitance $C = 0.05$ μF, and resistance $R = 160\ \Omega$. The initial value of the capacitor voltage is $v_c(t = 0) = V_{c0} = 0$ and conductor current $i(t = 0) = 0$. If switch S_1 is closed at $t = 0$, determine (a) an expression for the current $i(t)$, and (b) the conduction time of diode. (c) Draw a sketch of $i(t)$. (d) Use PSpice to plot the instantaneous current i for $R = 50\ \Omega$, $160\ \Omega$, and $320\ \Omega$.

Solution

a. From Eq. (2.40), $\alpha = R/2L = 160 \times 10^3/(2 \times 2) = 40{,}000$ rad/s, and from Eq. (2.41), $\omega_0 = 1/\sqrt{LC} = 10^5$ rad/s. The ringing frequency becomes

$$\omega_r = \sqrt{10^{10} - 16 \times 10^8} = 91{,}652 \text{ rad/s}$$

Because $\alpha < \omega_0$, it is an underdamped circuit and the solution is of the form

$$i(t) = e^{-\alpha t}(A_1 \cos \omega_r t + A_2 \sin \omega_r t)$$

At $t = 0$, $i(t = 0) = 0$ and this gives $A_1 = 0$. The solution becomes

$$i(t) = e^{-\alpha t} A_2 \sin \omega_r t$$

The derivative of $i(t)$ becomes

$$\frac{di}{dt} = \omega_r \cos \omega_r t A_2 e^{-\alpha t} - \alpha \sin \omega_r t A_2 e^{-\alpha}$$

When the switch is closed at $t = 0$, the capacitor offers a low impedance and the inductor offers a high impedance. The initial rate of rise of the current is limited only by the inductor L. Thus at $t = 0$, the circuit di/dt is V_s/L. Therefore,

$$\left.\frac{di}{dt}\right|_{t=0} = \omega_r A_2 = \frac{V_s}{L}$$

which gives the constant as

$$A_2 = \frac{V_s}{\omega_r L} = \frac{220 \times 1{,}000}{91{,}652 \times 2} = 1.2 \text{ A}$$

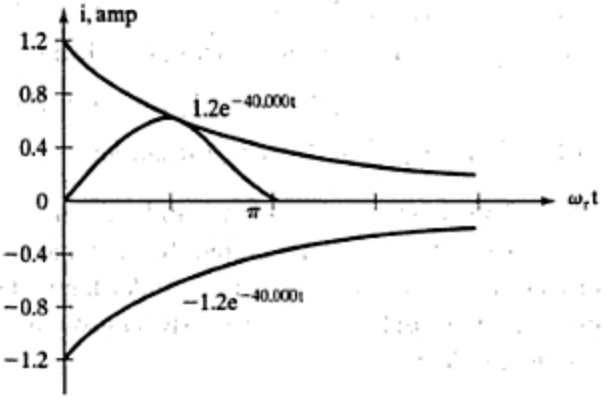


FIGURE 2.18
Current waveform for Example 2.6.

The final expression for the current $i(t)$ is

$$i(t) = 1.2 \sin(91{,}652t)e^{-40{,}000t}\text{A}$$

b. The conduction time t_1 of the diode is obtained when $i = 0$. That is,

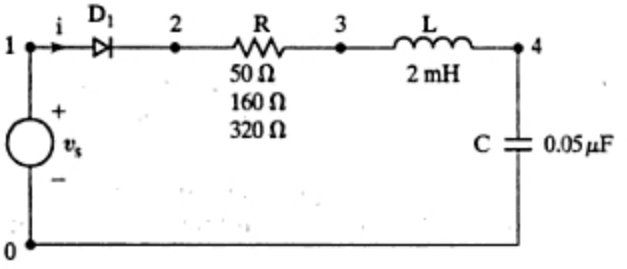
$$\omega_r t_1 = \pi \quad \text{or} \quad t_1 = \frac{\pi}{91{,}652} = 34.27\ \mu\text{s}$$

c. The sketch for the current waveform is shown in Figure 2.18.

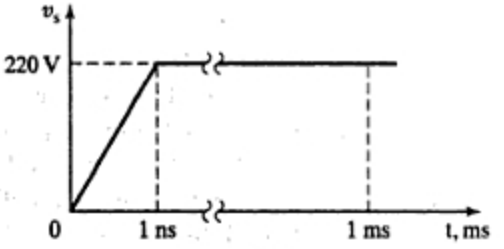
d. The circuit for PSpice simulation [4] is shown in Figure 2.19. The list of the circuit file is as follows:

```
Example 2.6        RLC Circuit with Diode
.PARAM  VALU = 160                          ;Define parameter VALU
.STEP   PARAM    VALU LIST 50 160 320       ; Vary parameter VALU
VS      1   0    PWL (0  0  INS 220V  1MS 220V) ; Piecewise linear
R       2   3    {VALU}                     ; Variable resistance
L       3   4    2MH
C       4   0    0.05UF
D1      1   2    DMOD                       ; Diode with model DMOD
.MODEL DMOD  D(IS=2.22E-15 BV=1800V)        ; Diode model parameters
.TRAN  0.1US  60US                          ; Transient analysis
.PROBE                                      ; Graphics postprocessor
.END
```

The PSpice plot of the current $I(R)$ through resistance R is shown in Figure 2.20. The current response depends on the resistance R. With a higher value of R, the current becomes more damped; and with a lower value, it tends more toward sinusoidal. For $R = 0$, the peak current becomes $V_s(C/L) = 220 \times (0.05\ \mu/2\text{m}) = 1.56$ A.



(a) Circuit



(b) Input voltage

FIGURE 2.19
RLC circuit for PSpice simulation.

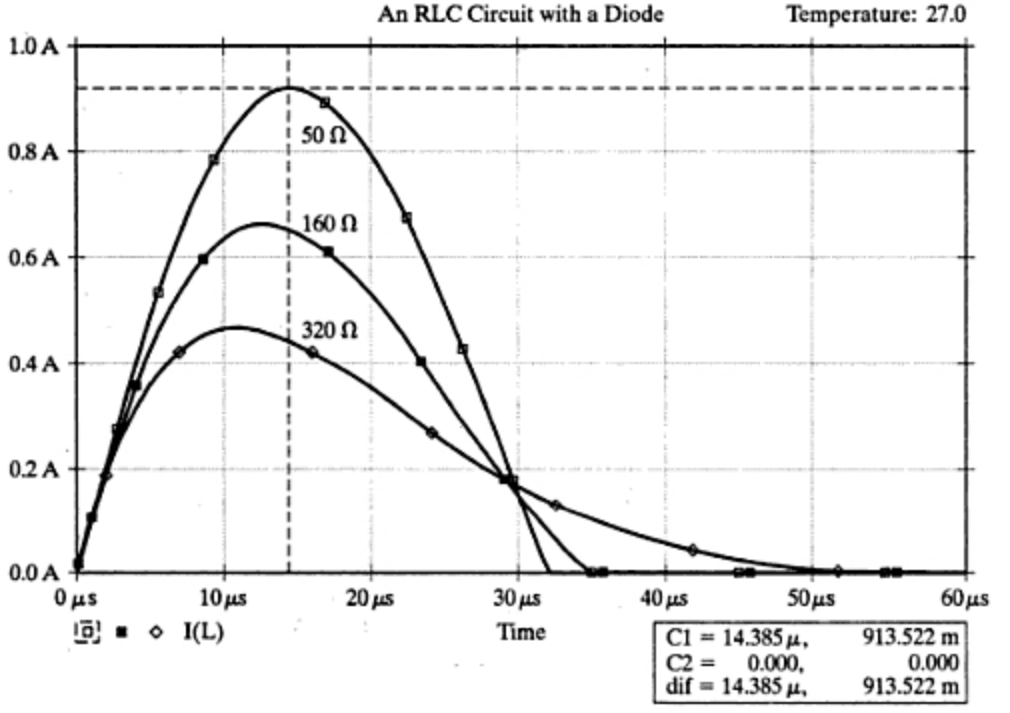


FIGURE 2.20
Plots for Example 2.6.

Key Points of Section 2.11

- The current of an LC circuit goes through resonant oscillation with a peak value of $V_s\ (C/L)$. The diode D_1 stops the reverse current flow and the capacitor is charged to $2V_s$.
- The current of an *RLC* depends on the damping ratio $\delta = (R/2)\,(C/L)$. Power electronics circuits are generally underdamped such that the circuit current becomes near sinusoidal.

2.12 FREEWHEELING DIODES

If switch S_1 in Figure 2.21a is closed for time t_1, a current is established through the load; and then if the switch is opened, a path must be provided for the current in the inductive load. Otherwise, the inductive energy induces a very high voltage and this energy is dissipated as heat across the switch as sparks. This is normally done by connecting a diode D_m as shown in Figure 2.21a, and this diode is usually called a *freewheeling diode*. The circuit operation can be divided into two modes. Mode 1 begins when the switch is closed at $t = 0$, and mode 2 begins when the switch is then opened. The equivalent circuits for the modes are shown in Figure 2.21b. Variables i_1

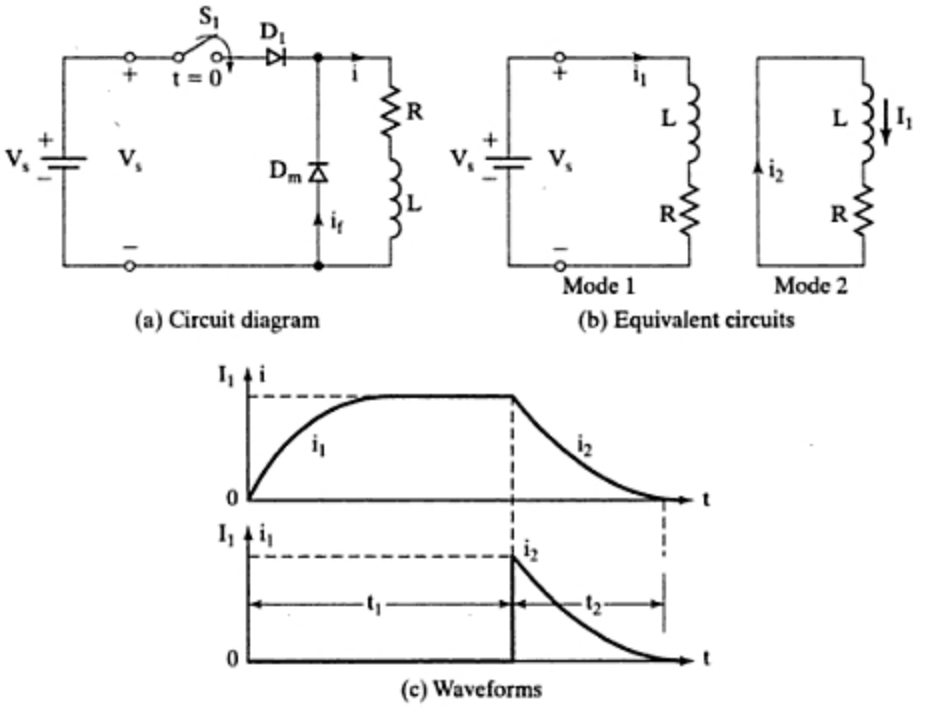


FIGURE 2.21

Circuit with a freewheeling diode.

and i_2 are defined as the instantaneous currents for mode 1 and mode 2, respectively, t_1 and t_2 are the corresponding durations of these modes.

Mode 1. During this mode, the diode current i_1, which is similar to Eq. (2.25), is

$$i_1(t) = \frac{V_s}{R}(1 - e^{-tR/L}) \tag{2.47}$$

When the switch is opened at $t = t_1$ (at the end of this mode), the current at that time becomes

$$I_1 = i_1(t = t_1) = \frac{V_s}{R}(1 - e^{t_1 R/L}) \tag{2.48}$$

If the time t_1 is sufficiently long, the current practically reaches a steady-state current of $I_s = V_s/R$ flows through the load.

Mode 2. This mode begins when the switch is opened and the load current starts to flow through the freewheeling diode D_m. Redefining the time origin at the beginning of this mode, the current through the freewheeling diode is found from

$$0 = L\frac{di_2}{dt} + Ri_2 \tag{2.49}$$

with initial condition $i_2(t = 0) = I_1$. The solution of Eq. (2.49) gives the freewheeling current $i_f = i_2$ as

$$i_2(t) = I_1 e^{-tR/L} \tag{2.50}$$

and at $t = t_2$ this current decays exponentially to practically zero provided that $t_2 \gg L/R$. The waveforms for the currents are shown in Figure 2.21c.

Note: Figure 2.21c shows that at t_1 and t_2, the currents have reached the steady-state conditions. These are the extreme cases. A circuit normally operates under conditions such that the current remains continuous.

Example 2.7 Finding the Stored Energy in an Inductor with a Freewheeling Diode

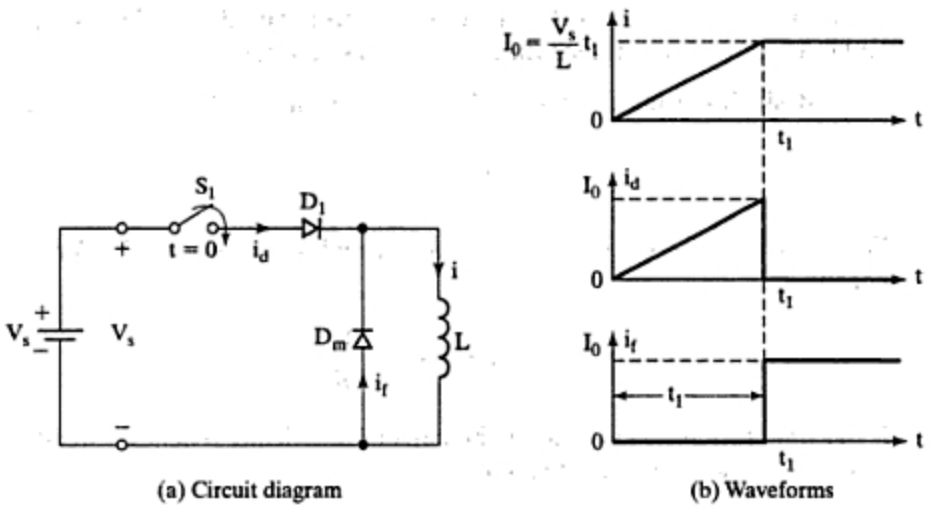
In Figure 2.21a, the resistance is negligible ($R = 0$), the source voltage is $V_s = 220$ V (constant time), and the load inductance is $L = 220$ μH. (a) Draw the waveform for the load current if the switch is closed for a time $t_1 = 100$ μs and is then opened. (b) Determine the final energy stored in the load inductor.

Solution

a. The circuit diagram is shown in Figure 2.22a with a zero initial current. When the switch is closed at $t = 0$, the load current rises linearly and is expressed as

$$i(t) = \frac{V_s}{L}t$$

and at $t = t_1$, $I_0 = V_s t_1/L = 220 \times 100/220 = 100$ A.



(a) Circuit diagram (b) Waveforms

FIGURE 2.22
Diode circuit with an L load.

b. When switch S_1 is opened at a time $t = t_1$, the load current starts to flow through diode D_m. Because there is no dissipative (resistive) element in the circuit, the load current remains constant at $I_0 = 100$ A and the energy stored in the inductor is $0.5LI_0^2 = 1.1$ J. The current waveforms are shown in Figure 2.22b.

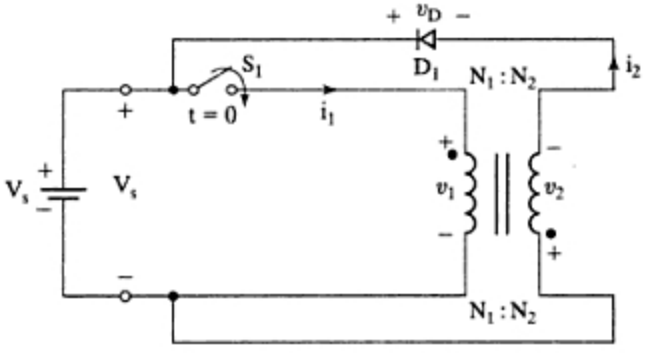
Key Points of Section 2.12

- If the load is inductive, an antiparallel diode known as the freewheeling diode must be connected across the load to provide a path for the inductive current to flow. Otherwise, energy may be trapped into an inductive load.

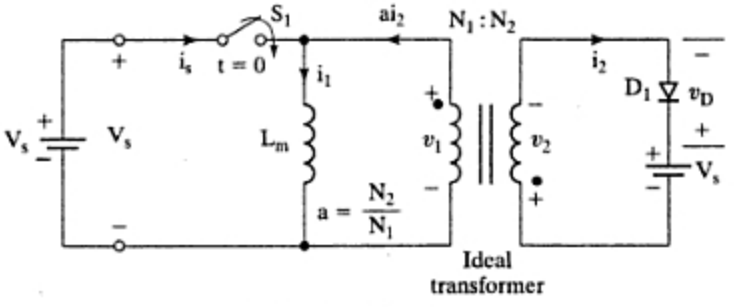
2.13 RECOVERY OF TRAPPED ENERGY WITH A DIODE

In the ideal lossless circuit [7] of Figure 2.22a, the energy stored in the inductor is trapped there because no resistance exists in the circuit. In a practical circuit it is desirable to improve the *efficiency* by returning the stored energy into the supply source. This can be achieved by adding to the inductor a second winding and connecting a diode D_1 as shown in Figure 2.23a. The inductor and the secondary winding behave as a transformer. The transformer secondary is connected such that if v_1 is positive, v_2 is negative with respect to v_1, and vice versa. The secondary winding that facilitates returning the stored energy to the source via diode D_1 is known as a *feedback winding*. Assuming a transformer with a magnetizing inductance of L_m, the equivalent circuit is as shown in Figure 2.23b.

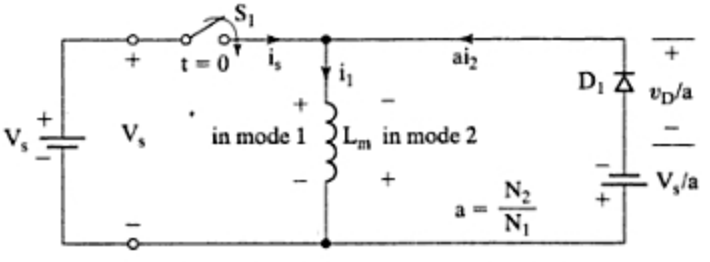
If the diode and secondary voltage (source voltage) are referred to the primary side of the transformer, the equivalent circuit is as shown in Figure 2.23c. Parameters i_1 and i_2 define the primary and secondary currents of the transformer, respectively.



(a) Circuit diagram



(b) Equivalent circuit



(c) Equivalent circuit, referred to primary side

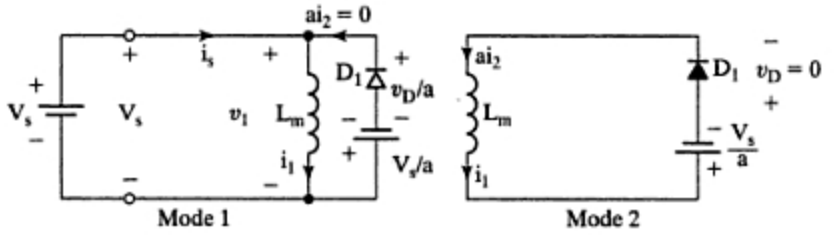
FIGURE 2.23

Circuit with an energy recovery diode. [Ref. 7, S. Dewan]

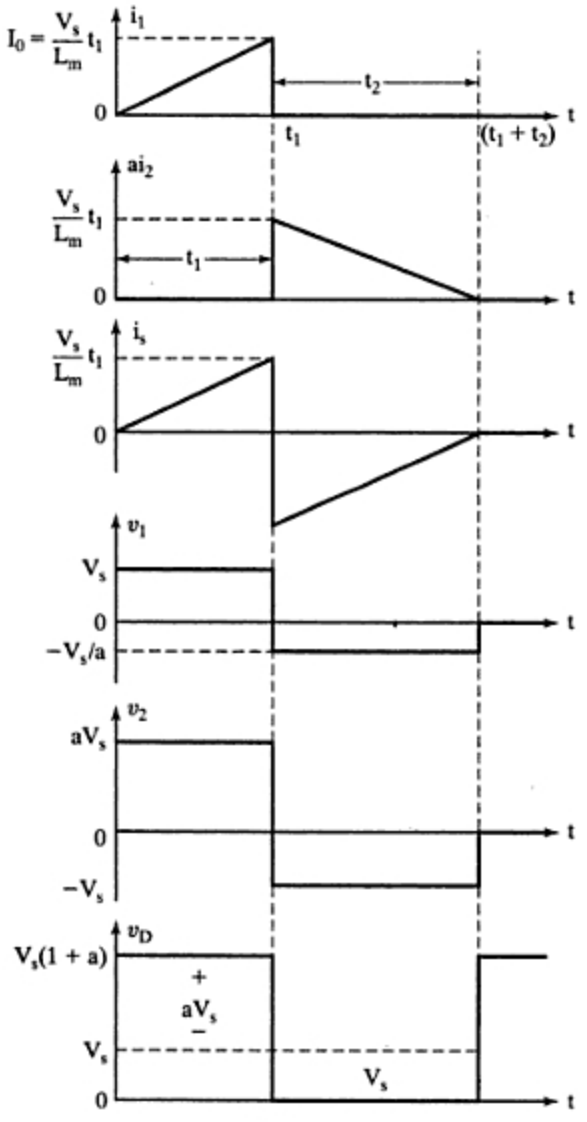
The *turns ratio* of an ideal transformer is defined as

$$a = \frac{N_2}{N_1} \tag{2.51}$$

The circuit operation can be divided into two modes. Mode 1 begins when switch S_1 is closed at $t = 0$ and mode 2 begins when the switch is opened. The equivalent circuits for the modes are shown in Figure 2.24a, with t_1 and t_2 the durations of mode 1 and mode 2, respectively.



(a) Equivalent circuit



(b) Waveforms

FIGURE 2.24

Equivalent circuits and waveforms.

Mode 1. During this mode switch S_1 is closed at $t = 0$. Diode D_1 is reverse biased and the current through the diode (secondary current) is $ai_2 = 0$ or $i_2 = 0$. Using the KVL in Figure 2.24a for mode 1, $V_s = (v_D - V_s)/a$, and this gives the reverse diode voltage as

$$v_D = V_s(1 + a) \tag{2.52}$$

Assuming that there is no initial current in the circuit, the primary current is the same as the switch current i_s and is expressed as

$$V_s = L_m \frac{di_1}{dt} \tag{2.53}$$

which gives

$$i_1(t) = i_s(t) = \frac{V_s}{L_m} t \quad \text{for} \quad 0 \le t \le t_1 \tag{2.54}$$

This mode is valid for $0 \le t \le t_1$ and ends when the switch is opened at $t = t_1$. At the end of this mode the primary current becomes

$$I_0 = \frac{V_s}{L_m} t_1 \tag{2.55}$$

Mode 2. During this mode the switch is opened, the voltage across the inductor is reversed, and the diode D_1 is forward biased. A current flows through the transformer secondary and the energy stored in the inductor is returned to the source. Using the KVL and redefining the time origin at the beginning of this mode, the primary current is expressed as

$$L_m \frac{di_1}{dt} + \frac{V_s}{a} = 0 \tag{2.56}$$

with initial condition $i_1(t = 0) = I_0$, and we can solve the current as

$$i_1(t) = -\frac{V_s}{aL_m} t + I_0 \quad \text{for} \quad 0 \le t \le t_2 \tag{2.57}$$

The conduction time of diode D_1 is found from the condition $i_1(t = t_2) = 0$ of Eq. (2.57) and is

$$t_2 = \frac{aL_m I_0}{V_s} = at_1 \tag{2.58}$$

Mode 2 is valid for $0 \le t \le t_2$. At the end of this mode at $t = t_2$, all the energy stored in the inductor L_m is returned to the source. The various waveforms for the currents and voltage are shown in Figure 2.24b for $a = 10/6$.

Example 2.8 Finding the Recovery Energy in an Inductor with a Feedback Diode

For the energy recovery circuit of Figure 2.23a, the magnetizing inductance of the transformer is $L_m = 250\ \mu H$, $N_1 = 10$, and $N_2 = 100$. The leakage inductances and resistances of the transformer are negligible. The source voltage is $V_s = 220$ V and there is no initial current in the circuit. If switch S_1 is closed for a time $t_1 = 50\ \mu s$ and is then opened, (a) determine the reverse voltage of diode D_1, (b) calculate the peak value of primary current, (c) calculate the peak value of secondary current, (d) determine the conduction time of diode D_1, and (e) determine the energy supplied by the source.

Solution

The turns ratio is $a = N_2/N_1 = 100/10 = 10$.

a. From Eq. (2.52) the reverse voltage of the diode,

$$v_D = V_s(1 + a) = 220 \times (1 + 10) = 2420\ \text{V}$$

b. From Eq. (2.55) the peak value of the primary current,

$$I_0 = \frac{V_s}{L_m} t_1 = 220 \times \frac{50}{250} = 44\ \text{A}$$

c. The peak value of the secondary current $I_0' = I_0/a = 44/10 = 4.4$ A.

d. From Eq. (2.58) the conduction time of the diode

$$t_2 = \frac{aL_m I_0}{V_s} = 250 \times 44 \times \frac{10}{220} = 500\ \mu s$$

e. The source energy,

$$W = \int_0^{t_1} vi\, dt = \int_0^{t_1} V_s \frac{V_s}{L_m} t\, dt = \frac{1}{2} \frac{V_s^2}{L_m} t_1^2$$

Using I_0 from Eq. (2.55) yields

$$W = 0.5 L_m I_0^2 = 0.5 \times 250 \times 10^{-6} \times 44^2 = 0.242\ \text{J} = 242\ \text{mJ}$$

Key Points of Section 2.13

- The trapped energy of an inductive load can be fed back to the input supply through a diode known as the feedback diode.

SUMMARY

The characteristics of practical diodes differ from those of ideal diodes. The reverse recovery time plays a significant role, especially at high-speed switching applications. Diodes can be classified into three types: (1) general-purpose diodes, (2) fast-recovery diodes, and (3) Schottky diodes. Although a Schottky diode behaves as a *pn*-junction

diode, there is no physical junction; and as a result a Schottky diode is a majority carrier device. On the other hand, a *pn*-junction diode is both a majority and a minority carrier diode.

If diodes are connected in series to increase the blocking voltage capability, voltage-sharing networks under steady-state and transient conditions are required. When diodes are connected in parallel to increase the current-carrying ability, current-sharing elements are also necessary.

In this chapter we have seen the applications of power diodes in voltage reversal of a capacitor, charging a capacitor more than the dc input voltage, freewheeling action, and energy recovery from an inductive load.

REFERENCES

[1] M. H. Rashid, *Microelectronic Circuits: Analysis and Design*. Boston: PWS Publishing. 1999, Chapter 2.

[2] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: John Wiley & Sons. 1993, Chapter 1.

[3] Infineon Technologies: *Power Semiconductors*. Germany: Siemens, 2001. www.infineon.com/

[4] M. H. Rashid, *SPICE for Circuits and Electronics Using PSpice*. Englewood Cliffs, NJ: Prentice-Hall Inc. 1995.

[5] M. H. Rashid, *SPICE for Power Electronics and Electric Power*. Englewood Cliffs, NJ: Prentice-Hall. 1993.

[6] P. W. Tuinenga, *SPICE: A guide to Circuit Simulation and Analysis Using PSpice*. Englewood Cliffs, NJ: Prentice-Hall. 1995.

[7] S. B. Dewan and A. Straughen, *Power Semiconductor Circuits*. New York: John Wiley & Sons. 1975, Chapter 2.

REVIEW QUESTIONS

2.1 What are the types of power diodes?
2.2 What is a leakage current of diodes?
2.3 What is a reverse recovery time of diodes?
2.4 What is a reverse recovery current of diodes?
2.5 What is a softness factor of diodes?
2.6 What are the recovery types of diodes?
2.7 What is the cause of reverse recovery time in a *pn*-junction diode?
2.8 What is the effect of reverse recovery time?
2.9 Why is it necessary to use fast-recovery diodes for high-speed switching?
2.10 What is a forward recovery time?
2.11 What are the main differences between *pn*-junction diodes and Schottky diodes?
2.12 What are the limitations of Schottky diodes?
2.13 What is the typical reverse recovery time of general-purpose diodes?
2.14 What is the typical reverse recovery time of fast-recovery diodes?
2.15 What are the problems of series-connected diodes, and what are the possible solutions?
2.16 What are the problems of parallel-connected diodes, and what are the possible solutions?
2.17 If two diodes are connected in series with equal-voltage sharings, why do the diode leakage currents differ?

2.18 What is the time constant of an *RL* circuit?
2.19 What is the time constant of an *RC* circuit?
2.20 What is the resonant frequency of an *LC* circuit?
2.21 What is the damping factor of an *RLC* circuit?
2.22 What is the difference between the resonant frequency and the ringing frequency of an *RLC* circuit?
2.23 What is a freewheeling diode, and what is its purpose?
2.24 What is the trapped energy of an inductor?
2.25 How is the trapped energy recovered by a diode?

PROBLEMS

2.1 The reverse recovery time of a diode is $t_{rr} = 5\ \mu s$, and the rate of fall of the diode current is $di/dt = 80\ A/\mu s$. If the softness factor is SF = 0.5, determine **(a)** the storage charge Q_{RR}, and **(b)** the peak reverse current I_{RR}.

2.2 The measured values of a diode at a temperature of 25 °C are

$$V_D = 1.0\ V \text{ at } I_D = 50\ A$$
$$= 1.5\ V \text{ at } I_D = 600\ A$$

Determine **(a)** the emission coefficient n, and **(b)** the leakage current I_s.

2.3 Two diodes are connected in series and the voltage across each diode is maintained the same by connecting a voltage-sharing resistor, such that $V_{D1} = V_{D2} = 2000\ V$ and $R_1 = 100\ k\Omega$. The $v-i$ characteristics of the diodes are shown in Figure P2.3. Determine the leakage currents of each diode and the resistance R_2 across diode D_2.

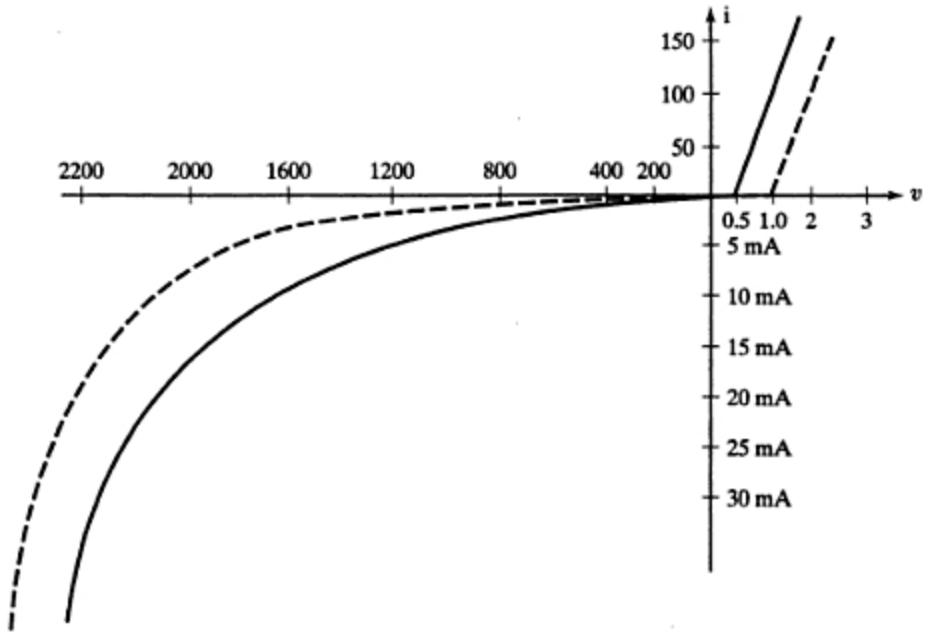


FIGURE P2.3

2.4 Two diodes are connected in parallel and the forward voltage drop across each diode is 1.5 V. The v–i characteristics of diodes are shown in Figure P2.3. Determine the forward currents through each diode.

2.5 Two diodes are connected in parallel as shown in Figure 2.11a, with current-sharing resistances. The v–i characteristics are shown in Figure P2.3. The total current is $I_T = 200$ A. The voltage across a diode and its resistance is $v = 2.5$ V. Determine the values of resistances R_1 and R_2 if the current is shared equally by the diodes.

2.6 Two diodes are connected in series as shown in Figure 2.8a. The resistance across the diodes is $R_1 = R_2 = 10\,\text{k}\Omega$. The input dc voltage is 5 kV. The leakage currents are $I_{s1} = 25$ mA and $I_{s2} = 40$ mA. Determine the voltage across the diodes.

2.7 The current waveforms of a capacitor are shown in Figure P2.7. Determine the average, root mean square (rms), and peak current ratings of the capacitor.

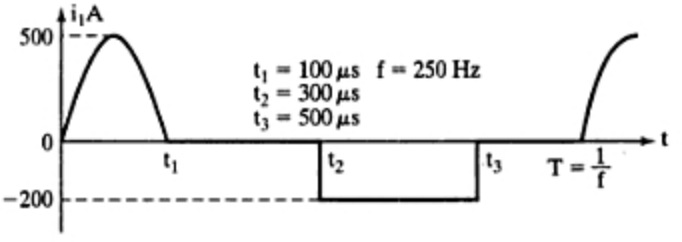


FIGURE P2.7

2.8 The waveforms of the current flowing through a diode are shown in Figure P2.8. Determine the average, rms, and peak current ratings of the diode.

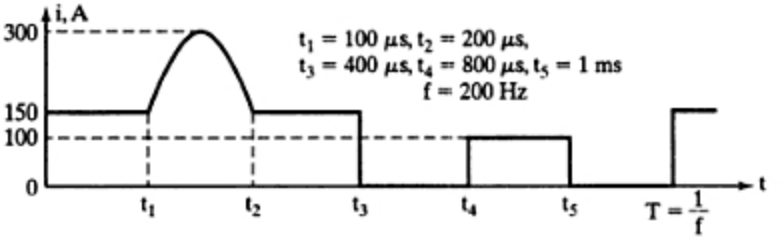


FIGURE P2.8

2.9 A diode circuit is shown in Figure P2.9 with $R = 22\ \Omega$ and $C = 10\ \mu$F. If switch S_1 is closed at $t = 0$, determine the expression for the voltage across the capacitor and the energy lost in the circuit.

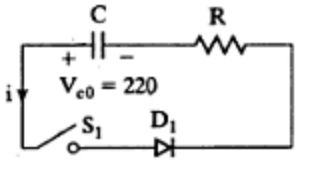


FIGURE P2.9

2.10 A diode circuit is shown in Figure P2.10 with $R = 10\ \Omega$, $L = 5$ mH, and $V_s = 220$ V. If a load current of 10 A is flowing through freewheeling diode D_m and switch S_1 is closed at $t = 0$, determine the expression for the current i through the switch.

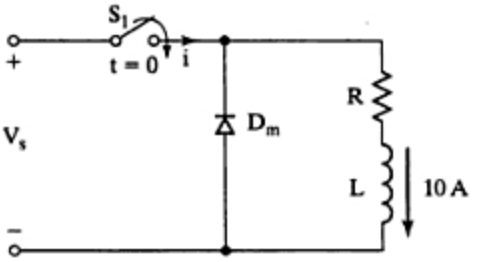


FIGURE P2.10

2.11 If the inductor of the circuit in Figure 2.15 has an initial current of I_0, determine the expression for the voltage across the capacitor.

2.12 If switch S_1 of Figure P2.12 is closed at $t = 0$, determine the expression for **(a)** the current flowing through the switch $i(t)$, and **(b)** the rate of rise of the current di/dt. **(c)** Draw sketches of $i(t)$ and di/dt. **(d)** What is the value of initial di/dt? For Figure P2.12e, find the initial di/dt only.

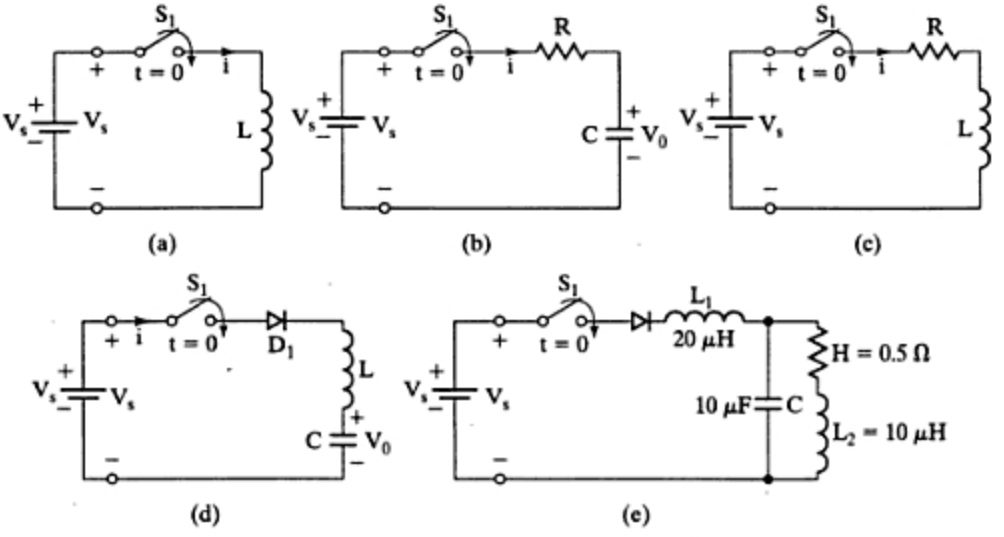


FIGURE P2.12

2.13 The second-order circuit of Figure 2.17 has the source voltage $V_s = 220$ V, inductance $L = 5$ mH, capacitance $C = 10\ \mu$F, and resistance $R = 22\ \Omega$. The initial voltage of the capacitor is $V_{c0} = 50$ V. If the switch is closed at $t = 0$, determine **(a)** an expression for the current, and **(b)** the conduction time of the diode. **(c)** Draw a sketch of $i(t)$.

2.14 For the energy recovery circuit of Figure 2.23a, the magnetizing inductance of the transformer is $L_m = 150\,\mu H$, $N_1 = 10$, and $N_2 = 200$. The leakage inductances and resistances of the transformer are negligible. The source voltage is $V_s = 200$ V and there is no initial current in the circuit. If switch S_1 is closed for a time $t_1 = 100\,\mu s$ and is then opened, **(a)** determine the reverse voltage of diode D_1, **(b)** calculate the peak primary current, **(c)** calculate the peak secondary current, **(d)** determine the time for which diode D_1 conducts, and **(e)** determine the energy supplied by the source.

2.15 A diode circuit is shown in Figure P2.15 where the load current is flowing through diode D_m. If switch S_1 is closed at a time $t = 0$, determine **(a)** expressions for $v_c(t)$, $i_c(t)$, and $i_d(t)$; **(b)** time t_1 when the diode D_1 stops conducting; **(c)** time t_q when the voltage across the capacitor becomes zero; and **(d)** the time required for capacitor to recharge to the supply voltage V_s.

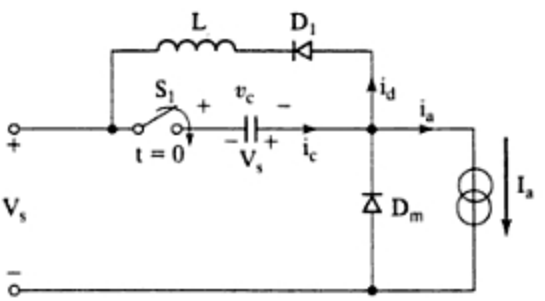


FIGURE P2.15

CHAPTER 3

Diode Rectifiers

The learning objectives of this chapter are as follows:

- To understand the operation and characteristics of diode rectifiers
- To learn the types of diode rectifiers
- To understand the performance parameters of diode rectifiers
- To learn the techniques for analyzing and design of diode rectifier circuits
- To learn the techniques for simulating diode rectifiers by using SPICE
- To study the effects of load inductance on the load current

3.1 INTRODUCTION

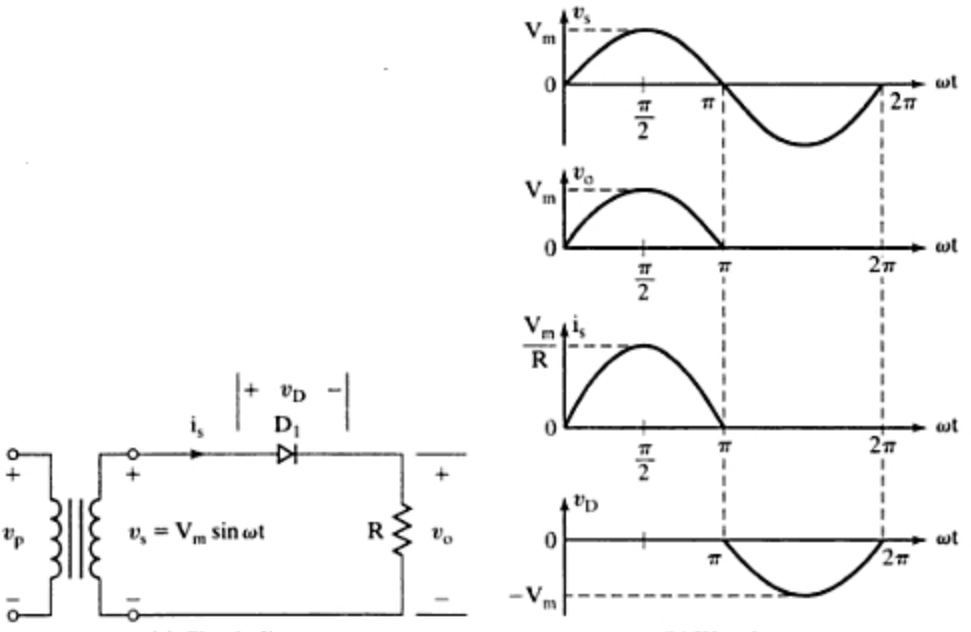
Diodes are extensively used in rectifiers. A *rectifier* is a circuit that converts an ac signal into a unidirectional signal. A rectifier is a type of dc–ac converter. Depending on the type of input supply, the rectifiers are classified into two types: (1) single phase and (2) three phase. For the sake of simplicity the diodes are considered to be ideal. By "ideal" we mean that the reverse recovery time t_{rr} and the forward voltage drop V_D are negligible. That is, $t_{rr} = 0$ and $V_D = 0$.

3.2 SINGLE-PHASE HALF-WAVE RECTIFIERS

A single-phase half-wave rectifier is the simplest type, but it is not normally used in industrial applications. However, it is useful in understanding the principle of rectifier operation. The circuit diagram with a resistive load is shown in Figure 3.1a. During the positive half-cycle of the input voltage, diode D_1 conducts and the input voltage appears across the load. During the negative half-cycle of the input voltage, the diode is in a *blocking condition* and the output voltage is zero. The waveforms for the input voltage and output voltage are shown in Figure 3.1b.

Key Points of Section 3.2

- The half-wave rectifier is the simplest power electronics circuit that is used for low-cost power supplies for electronics like radios.



(a) Circuit diagram (b) Waveforms

FIGURE 3.1

Single-phase half-wave rectifier.

3.3 PERFORMANCE PARAMETERS

Although the output voltage as shown in Figure 3.1b is dc, it is discontinuous and contains harmonics. A rectifier is a power processor that should give a dc output voltage with a minimum amount of harmonic contents. At the same time, it should maintain the input current as sinusoidal as possible and in phase with the input voltage so that the power factor is near unity. The power-processing quality of a rectifier requires the determination of harmonic contents of the input current, the output voltage, and the output current. We can use Fourier series expansions to find the harmonic contents of voltages and currents. There are different types of rectifier circuits and the performances of a rectifier are normally evaluated in terms of the following parameters:

The *average* value of the output (load) voltage, V_{dc}
The average value of the output (load) current, I_{dc}
The output dc power,

$$P_{dc} = V_{dc} I_{dc} \tag{3.1}$$

The root-mean-square (rms) value of the output voltage, V_{rms}
The rms value of the output current, I_{rms}

The output ac power

$$P_{ac} = V_{rms} I_{rms} \tag{3.2}$$

The *efficiency* (or *rectification ratio*) of a rectifier, which is a figure of merit and permits us to compare the effectiveness, is defined as

$$\eta = \frac{P_{dc}}{P_{ac}} \tag{3.3}$$

The output voltage can be considered as composed of two components: (1) the dc value, and (2) the ac component or ripple.

The *effective* (rms) value of the ac component of output voltage is

$$V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2} \tag{3.4}$$

The *form factor*, which is a measure of the shape of output voltage, is

$$FF = \frac{V_{rms}}{V_{dc}} \tag{3.5}$$

The *ripple factor*, which is a measure of the ripple content, is defined as

$$RF = \frac{V_{ac}}{V_{dc}} \tag{3.6}$$

Substituting Eq. (3.4) in Eq. (3.6), the ripple factor can be expressed as

$$RF = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} = \sqrt{FF^2 - 1} \tag{3.7}$$

The *transformer utilization factor* is defined as

$$TUF = \frac{P_{dc}}{V_s I_s} \tag{3.8}$$

where V_s and I_s are the rms voltage and rms current of the transformer secondary, respectively. Let us consider the waveforms of Figure 3.2, where v_s is the sinusoidal input voltage, i_s is the instantaneous input current, and i_{s1} is its fundamental component.

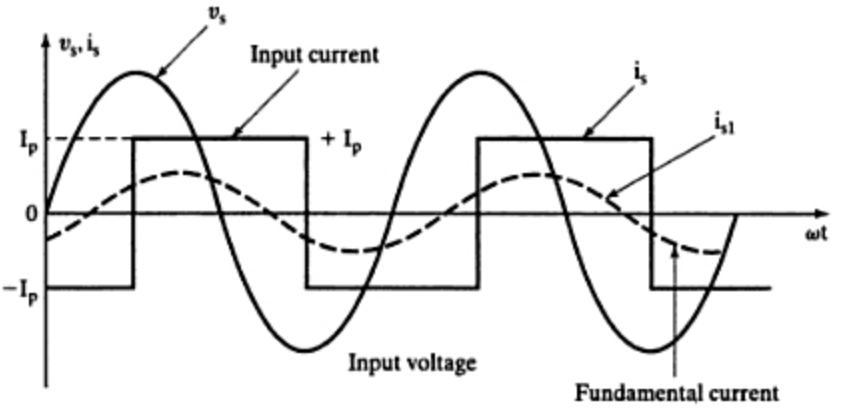


FIGURE 3.2

Waveforms for input voltage and current.

If ϕ is the angle between the fundamental components of the input current and voltage, ϕ is called the *displacement angle*. The *displacement factor* is defined as

$$\text{DF} = \cos\phi \tag{3.9}$$

The *harmonic factor* (HF) of the input current is defined as

$$\text{HF} = \left(\frac{I_s^2 - I_{s1}^2}{I_{s1}^2}\right)^{1/2} = \left[\left(\frac{I_s}{I_{s1}}\right)^2 - 1\right]^{1/2} \tag{3.10}$$

where I_{s1} is the fundamental component of the input current I_s. Both I_{s1} and I_s are expressed here in rms. The input *power factor* (PF) is defined as

$$\text{PF} = \frac{V_s I_{s1}}{V_s I_s}\cos\phi = \frac{I_{s1}}{I_s}\cos\phi \tag{3.11}$$

Crest factor (CF), which is a measure of the peak input current $I_{s(\text{peak})}$ as compared with its rms value I_s, is often of interest to specify the peak current ratings of devices and components. CF of the input current is defined by

$$\text{CF} = \frac{I_{s(\text{peak})}}{I_s} \tag{3.12}$$

Notes

1. HF is a measure of the distortion of a waveform and is also known as *total harmonic distortion* (THD).
2. If the input current i_s is purely sinusoidal, $I_{s1} = I_s$ and the power factor PF equals the displacement factor DF. The displacement angle ϕ becomes the impedance angle $\theta = \tan^{-1}(\omega L/R)$ for an RL load.
3. Displacement factor DF is often known as *displacement power factor* (DPF).
4. An ideal rectifier should have $\eta = 100\%$, $V_{\text{ac}} = 0$, RF = 0, TUF = 1, HF = THD = 0, and PF = DPF = 1.

Example 3.1 Finding the Performance Parameters of a Half-Wave Rectifier

The rectifier in Figure 3.1a has a purely resistive load of R. Determine (a) the efficiency, (b) the FF, (c) the RF, (d) the TUF, (e) the PIV of diode D_1, (f) the CF of the input current, and (g) input PF.

Solution

The average output voltage V_{dc} is defined as

$$V_{\text{dc}} = \frac{1}{T}\int_0^T v_L(t)\,dt$$

We can notice from Figure 3.1b that $v_L(t) = 0$ for $T/2 \le t \le T$. Hence, we have

$$V_{\text{dc}} = \frac{1}{T}\int_0^{T/2} V_m \sin\omega t\,dt = \frac{-V_m}{\omega T}\left(\cos\frac{\omega T}{2} - 1\right)$$

However, the frequency of the source is $f = 1/T$ and $\omega = 2\pi f$. Thus

$$V_{dc} = \frac{V_m}{\pi} = 0.318V_m$$
$$I_{dc} = \frac{V_{dc}}{R} = \frac{0.318V_m}{R} \tag{3.13}$$

The rms value of a periodic waveform is defined as

$$V_{rms} = \left[\frac{1}{T}\int_0^T v_L^2(t)\,dt\right]^{1/2}$$

For a sinusoidal voltage of $v_0(t) = V_m \sin \omega t$ for $0 \le t \le T/2$, the rms value of the output voltage is

$$V_{rms} = \left[\frac{1}{T}\int_0^{T/2} (V_m \sin \omega t)^2\,dt\right]^{1/2} = \frac{V_m}{2} = 0.5V_m$$
$$I_{rms} = \frac{V_{rms}}{R} = \frac{0.5V_m}{R} \tag{3.14}$$

From Eq. (3.1), $P_{dc} = (0.318V_m)^2/R$, and from Eq. (3.2), $P_{ac} = (0.5V_m)^2/R$.

a. From Eq. (3.3), the efficiency $\eta = (0.318V_m)^2/(0.5V_m)^2 = 40.5\%$.

b. From Eq. (3.5), the FF $= 0.5V_m/0.318V_m = 1.57$ or 157%.

c. From Eq. (3.7), the RF $= \sqrt{1.57^2 - 1} = 1.21$ or 121%.

d. The rms voltage of the transformer secondary is

$$V_s = \left[\frac{1}{T}\int_0^T (V_m \sin \omega t)^2\,dt\right]^{1/2} = \frac{V_m}{\sqrt{2}} = 0.707V_m \tag{3.15}$$

The rms value of the transformer secondary current is the same as that of the load:

$$I_s = \frac{0.5V_m}{R}$$

The *volt-ampere* rating (VA) of the transformer, VA $= V_s I_s = 0.707V_m \times 0.5V_m/R$. From Eq. (3.8) TUF $= P_{ac}/(V_s I_s) = 0.318^2/(0.707 \times 0.5) = 0.286$.

e. The peak reverse (or inverse) blocking voltage PIV $= V_m$.

f. $I_{s(peak)} = V_m/R$ and $I_s = 0.5V_m/R$. The CF of the input current is CF $= I_{s(peak)}/I_s = 1/0.5 = 2$.

g. The input PF for a resistive load can be found from

$$\text{PF} = \frac{P_{ac}}{\text{VA}} = \frac{0.5^2}{0.707 \times 0.5} = 0.707$$

Note: 1/TUF = 1/0.286 = 3.496 signifies that the transformer must be 3.496 times larger than that when it is used to deliver power from a pure ac voltage. This rectifier has a high ripple factor, 121%; a low efficiency, 40.5%; and a poor TUF, 0.286. In addition, the transformer has to carry a dc current, and this results in a dc saturation problem of the transformer core.

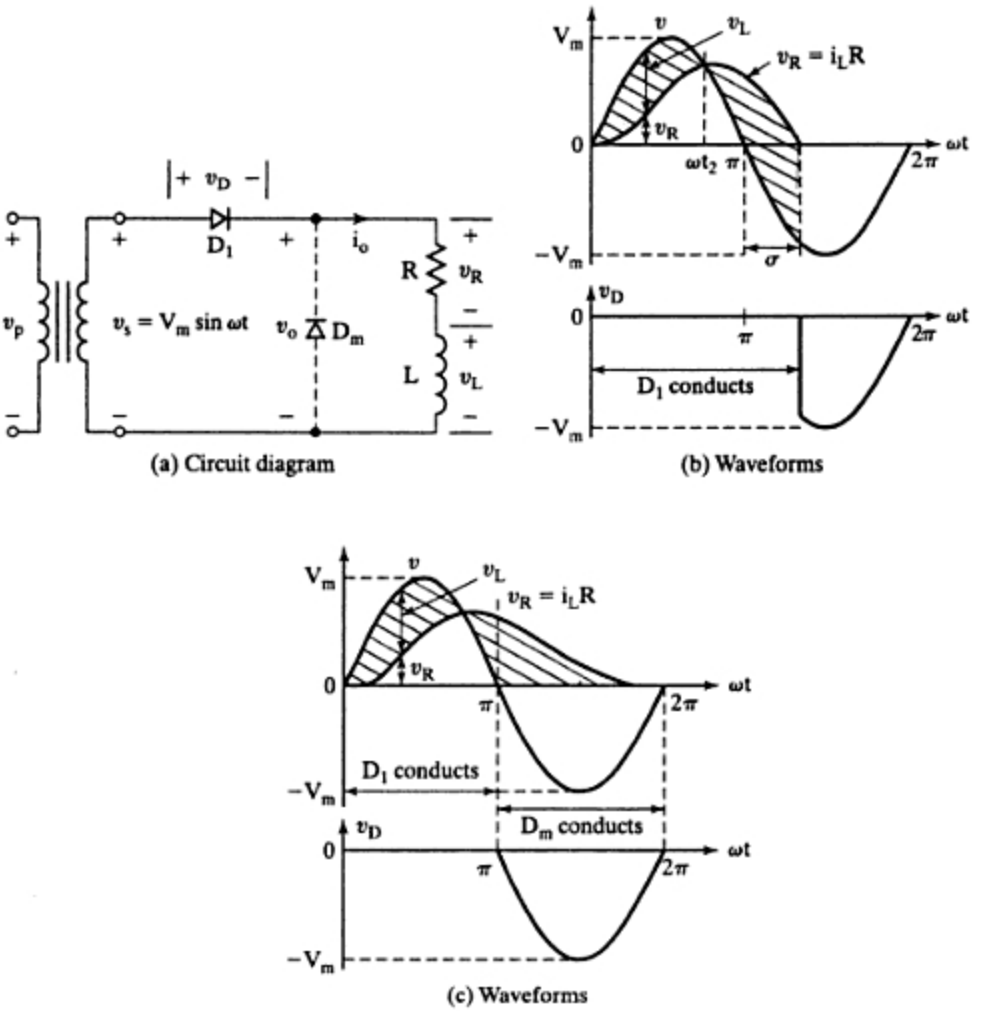


FIGURE 3.3

Half-wave rectifier with *RL* load.

Let us consider the circuit of Figure 3.1a with an *RL* load as shown in Figure 3.3a. Due to inductive load, the conduction period of diode D_1 will extend beyond 180° until the current becomes zero at $\omega t = \pi + \sigma$. The waveforms for the current and voltage are shown in Figure 3.3b. It should be noted that the average v_L of the inductor is zero. The average output voltage is

$$V_{dc} = \frac{V_m}{2\pi}\int_0^{\pi+\sigma} \sin \omega t \, d(\omega t) = \frac{V_m}{2\pi}[-\cos \omega t]_0^{\pi+\sigma}$$

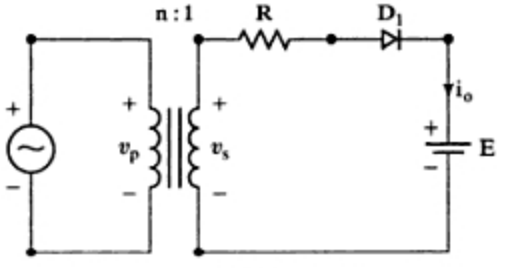
$$= \frac{V_m}{2\pi}[1 - \cos(\pi + \sigma)] \tag{3.16}$$

The average load current is $I_{dc} = V_{dc}/R$.

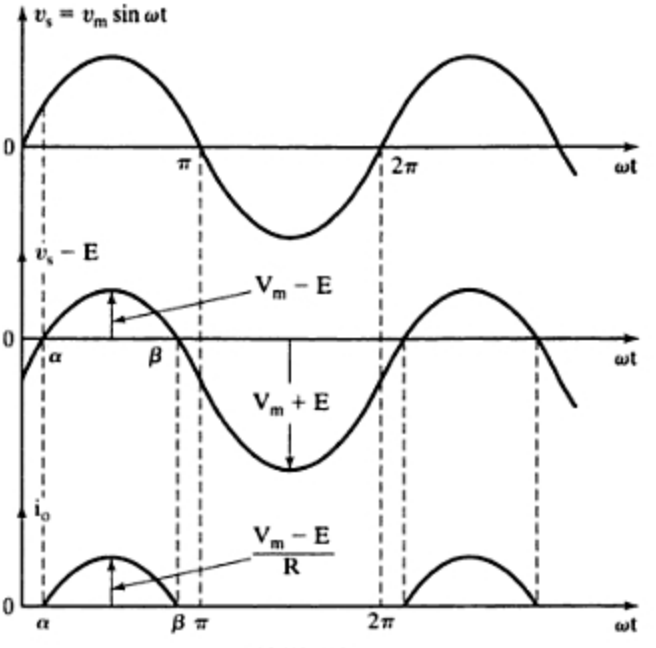
It can be noted from Eq. (3.16) that the average voltage (and current) can be increased by making $\sigma = 0$, which is possible by adding a freewheeling diode D_m as shown in Figure 3.3a with dashed lines. The effect of this diode is to prevent a negative voltage appearing across the load; and as a result, the magnetic stored energy is increased. At $t = t_1 = \pi/\omega$, the current from D_1 is transferred to D_m and this process is called *commutation* of diodes and the waveforms are shown in Figure 3.3c. Depending on the load time constant, the load current may be discontinuous. Load current i_0 is discontinuous with a resistive load and continuous with a very high inductive load. The continuity of the load current depends on its time constant $\tau = \omega L/R$.

If the output is connected to a battery, the rectifier can be used as a battery charger. This is shown in Figure 3.4a. For $v_s > E$, diode D_1 conducts. The angle α when the diode starts conducting can be found from the condition

$$V_m \sin \alpha = E$$



(a) Circuit



(b) Waveforms

FIGURE 3.4
Battery charger.

which gives

$$\alpha = \sin^{-1}\frac{E}{V_m} \tag{3.17}$$

Diode D_1 is turned off when $v_s < E$ at

$$\beta = \pi - \alpha$$

The charging current i_L, which is shown in Figure 3.4b, can be found from

$$i_0 = \frac{v_s - E}{R} = \frac{V_m \sin \omega t - E}{R} \qquad \text{for } \alpha < \omega t < \beta$$

Example 3.2 Finding the Performance Parameters of a Battery Charger

The battery voltage in Figure 3.4a is $E = 12$ V and its capacity is 100 Wh. The average charging current should be $I_{dc} = 5$ A. The primary input voltage is $V_p = 120$ V, 60 Hz, and the transformer has a turn ratio of $n = 2{:}1$. Calculate (a) the conduction angle δ of the diode, (b) the current-limiting resistance R, (c) the power rating P_R of R, (d) the charging time h_o in hours, (e) the rectifier efficiency η, and (f) the PIV of the diode.

Solution

$E = 12$ V, $V_p = 120$ V, $V_s = V_p/n = 120/2 = 60$ V, and $V_m = \sqrt{2}\,V_s = \sqrt{2} \times 60 = 84.85$ V.

a. From Eq. (3.17), $\alpha = \sin^{-1}(12/84.85) = 8.13°$ or 0.1419 rad. $\beta = 180 - 8.13 = 171.87°$. The conduction angle is $\delta = \beta - \alpha = 171.87 - 8.13 = 163.74°$.

b. The average charging current I_{dc} is

$$I_{dc} = \frac{1}{2\pi}\int_{\alpha}^{\beta}\frac{V_m \sin \omega t - E}{R}\, d(\omega t)$$

$$= \frac{1}{2\pi R}(2V_m \cos \alpha + 2E\alpha - \pi E), \text{ for } \beta = \pi - \alpha \tag{3.18}$$

which gives

$$R = \frac{1}{2\pi I_{dc}}(2V_m \cos \alpha + 2E\alpha - \pi E)$$

$$= \frac{1}{2\pi \times 5}(2 \times 84.85 \times \cos 8.13° + 2 \times 12 \times 0.1419 - \pi \times 12) = 4.26\ \Omega$$

c. The rms battery current I_{rms} is

$$I_{rms}^2 = \frac{1}{2\pi}\int_{\alpha}^{\beta}\frac{(V_m \sin \omega t - E)^2}{R^2}\, d(\omega t)$$

$$= \frac{1}{2\pi R^2}\left[\left(\frac{V_m^2}{2} + E^2\right)(\pi - 2\alpha) + \frac{V_m^2}{2}\sin 2\alpha - 4V_m E \cos \alpha\right]$$

$$= 67.4 \tag{3.19}$$

or $I_{rms} = \sqrt{67.4} = 8.2$ A. The power rating of R is $P_R = 8.2^2 \times 4.26 = 286.4$ W.

d. The power delivered P_{dc} to the battery is

$$P_{dc} = EI_{dc} = 12 \times 5 = 60 \text{ W}$$
$$h_o P_{dc} = 100 \quad \text{or} \quad h_o = \frac{100}{P_{dc}} = \frac{100}{60} = 1.667 \text{ h}$$

e. The rectifier efficiency η is

$$\eta = \frac{\text{power delivered to the battery}}{\text{total input power}} = \frac{P_{dc}}{P_{dc} + P_R} = \frac{60}{60 + 286.4} = 17.32\%$$

f. The peak inverse voltage PIV of the diode is

$$\text{PIV} = V_m + E$$
$$= 84.85 + 12 = 96.85 \text{ V}$$

Example 3.3 Finding the Fourier Series of the Output Voltage for a Half-Wave Rectifier

The single-phase half-wave rectifier of Figure 3.1a is connected to a source of $V_s = 120$ V, 60 Hz. Express the instantaneous output voltage $v_0(t)$ in Fourier series.

Solution

The rectifier output voltage v_0 may be described by a Fourier series as

$$v_0(t) = V_{dc} + \sum_{n=1,2,\ldots}^{\infty} (a_n \sin n\omega t + b_n \cos n\omega t)$$

$$V_{dc} = \frac{1}{2\pi}\int_0^{2\pi} v_0 \, d(\omega t) = \frac{1}{2\pi}\int_0^{\pi} V_m \sin \omega t \, d(\omega t) = \frac{V_m}{\pi}$$

$$a_n = \frac{1}{\pi}\int_0^{2\pi} v_0 \sin n\omega t \, d(\omega t) = \frac{1}{\pi}\int_0^{\pi} V_m \sin \omega t \sin n\omega t \, d(\omega t)$$
$$= \frac{V_m}{2} \qquad \text{for } n = 1$$
$$= 0 \qquad \text{for } n = 2, 3, 4, 5, 6, \ldots$$

$$b_n = \frac{1}{\pi}\int_0^{2\pi} v_0 \cos n\omega t \, d(\omega t) = \frac{1}{\pi}\int_0^{\pi} V_m \sin \omega t \cos n\omega t \, d(\omega t)$$
$$= \frac{V_m}{\pi}\frac{1 + (-1)^n}{1 - n^2} \qquad \text{for } n = 2, 4, 6, \ldots$$
$$= 0 \qquad \text{for } n = 1, 3, 5, \ldots$$

Substituting a_n and b_n, the instantaneous output voltage becomes

$$v_0(t) = \frac{V_m}{\pi} + \frac{V_m}{2}\sin \omega t - \frac{2V_m}{3\pi}\cos 2\omega t - \frac{2V_m}{15\pi}\cos 4\omega t - \frac{2V_m}{35\pi}\cos 6\omega t - \cdots \qquad (3.20)$$

where $V_m = \sqrt{2} \times 120 = 169.7$ V and $\omega = 2\pi \times 60 = 377$ rad/s.

Key Points of Section 3.3

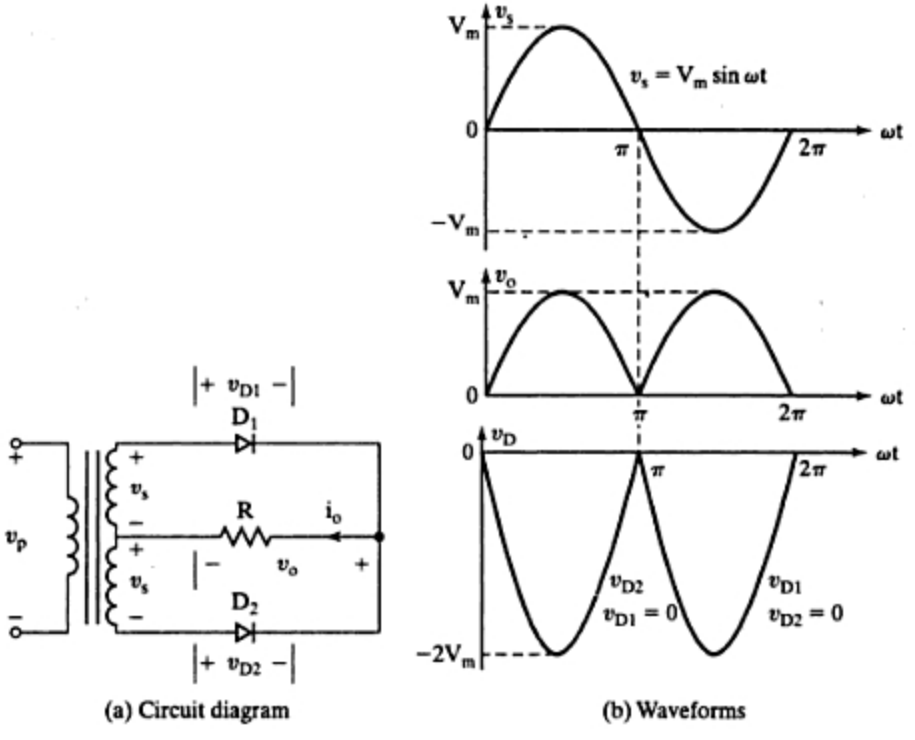
- The performance of a half-wave rectifier that is measured by certain parameters is poor. The load current can be made continuous by adding an inductor and a freewheeling diode. The output voltage is discontinuous and contains harmonics at multiples of the supply frequency.

3.4 SINGLE-PHASE FULL-WAVE RECTIFIERS

A full-wave rectifier circuit with a center-tapped transformer is shown in Figure 3.5a. Each half of the transformer with its associated diode acts as a half-wave rectifier and the output of a full-wave rectifier is shown in Figure 3.5b. Because there is no dc current flowing through the transformer, there is no dc saturation problem of transformer core. The average output voltage is

$$V_{dc} = \frac{2}{T}\int_0^{T/2} V_m \sin \omega t \, dt = \frac{2V_m}{\pi} = 0.6366V_m \tag{3.21}$$

Instead of using a center-tapped transformer, we could use four diodes, as shown in Figure 3.6a. During the positive half-cycle of the input voltage, the power is supplied



(a) Circuit diagram (b) Waveforms

FIGURE 3.5
Full-wave rectifier with center-tapped transformer.

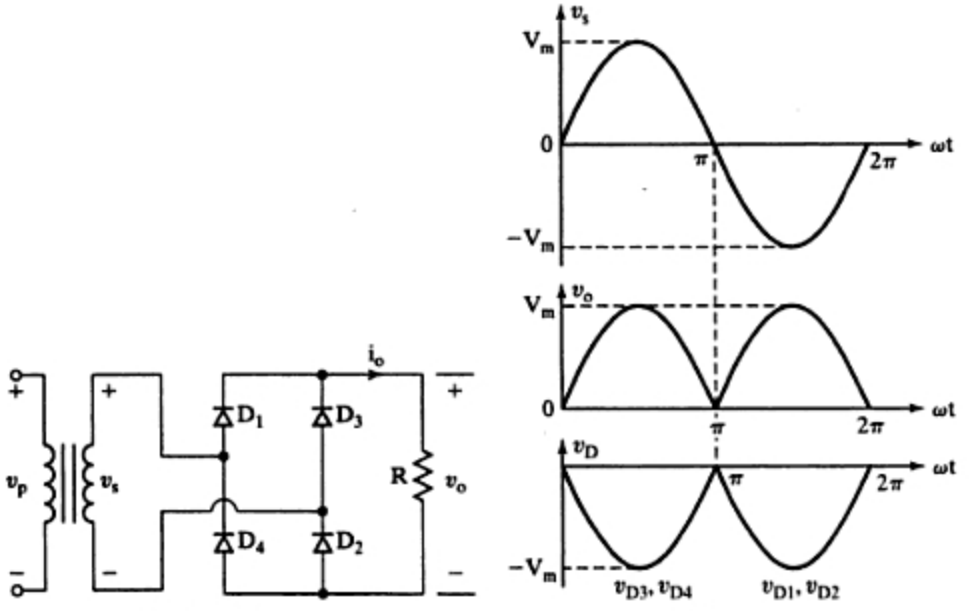


FIGURE 3.6
Full-wave bridge rectifier.

to the load through diodes D_1 and D_2. During the negative cycle, diodes D_3 and D_4 conduct. The waveform for the output voltage is shown in Figure 3.6b and is similar to that of Figure 3.5b. The peak-inverse voltage of a diode is only V_m. This circuit is known as a *bridge rectifier*, and it is commonly used in industrial applications [1, 2].

Example 3.4 Finding the Performance Parameters of a Full-Wave Rectifier with Center-Tapped Transformer

If the rectifier in Figure 3.5a has a purely resistive load of R, determine (a) the efficiency, (b) the FF, (c) the RF, (d) the TUF, (e) the PIV of diode D_1, and (f) the CF of the input current.

Solution

From Eq. (3.21), the average output voltage is

$$V_{dc} = \frac{2V_m}{\pi} = 0.6366V_m$$

and the average load current is

$$I_{dc} = \frac{V_{dc}}{R} = \frac{0.6366V_m}{R}$$

The rms value of the output voltage is

$$V_{\text{rms}} = \left[\frac{2}{T}\int_0^{T/2} (V_m \sin \omega t)^2\, dt\right]^{1/2} = \frac{V_m}{\sqrt{2}} = 0.707V_m$$

$$I_{\text{rms}} = \frac{V_{\text{rms}}}{R} = \frac{0.707V_m}{R}$$

From Eq. (3.1) $P_{\text{dc}} = (0.6366V_m)^2/R$, and from Eq. (3.2) $P_{\text{ac}} = (0.707V_m)^2/R$.

a. From Eq. (3.3), the efficiency $\eta = (0.6366V_m)^2/(0.707V_m)^2 = 81\%$.

b. From Eq. (3.5), the form factor $\text{FF} = 0.707V_m/0.6366V_m = 1.11$.

c. From Eq. (3.7), the ripple factor $\text{RF} = \sqrt{1.11^2 - 1} = 0.482$ or 48.2%.

d. The rms voltage of the transformer secondary $V_s = V_m/\sqrt{2} = 0.707V_m$. The rms value of transformer secondary current $I_s = 0.5V_m/R$. The volt-ampere rating (VA) of the transformer, $\text{VA} = 2V_sI_s = 2 \times 0.707V_m \times 0.5V_m/R$. From Eq. (3.8),

$$\text{TUF} = \frac{0.6366^2}{2 \times 0.707 \times 0.5} = 0.5732 = 57.32\%$$

e. The peak reverse blocking voltage, $\text{PIV} = 2V_m$.

f. $I_{s(\text{peak})} = V_m/R$ and $I_s = 0.707V_m/R$. The CF of the input current is $\text{CF} = I_{s(\text{peak})}/I_s = 1/0.707 = \sqrt{2}$.

g. The input PF for a resistive load can be found from

$$\text{PF} = \frac{P_{\text{ac}}}{\text{VA}} = \frac{0.707^2}{2 \times 0.707 \times 0.5} = 0.707$$

Note: 1/TUF = 1/0.5732 = 1.75 signifies that the input transformer, if present, must be 1.75 times larger than that when it is used to deliver power from a pure ac sinusoidal voltage. The rectifier has an RF of 48.2% and a rectification efficiency of 81%.

Note: The performance of a full-wave rectifier is significantly improved compared with that of a half-wave rectifier.

Example 3.5 Finding the Fourier Series of the Output Voltage for a Full-Wave Rectifier

The rectifier in Figure 3.5a has an *RL* load. Use the method of Fourier series to obtain expressions for output voltage $v_0(t)$.

Solution

The rectifier output voltage may be described by a Fourier series (which is reviewed in Appen dix E) as

$$v_0(t) = V_{\text{dc}} + \sum_{n=2,4,\ldots}^{\infty} (a_n \cos n\omega t + b_n \sin n\omega t)$$

where

$$V_{dc} = \frac{1}{2\pi}\int_0^{2\pi} v_0(t)\, d(\omega t) = \frac{2}{2\pi}\int_0^{\pi} V_m \sin \omega t\, d(\omega t) = \frac{2V_m}{\pi}$$

$$a_n = \frac{1}{\pi}\int_0^{2\pi} v_0 \cos n\omega t\, d(\omega t) = \frac{2}{\pi}\int_0^{\pi} V_m \sin \omega t \cos n\omega t\, d(\omega t)$$

$$= \frac{4V_m}{\pi} \sum_{n=2,4,\ldots}^{\infty} \frac{-1}{(n-1)(n+1)} \qquad \text{for } n = 2, 4, 6, \ldots$$

$$= 0 \qquad \text{for } n = 1, 3, 5, \ldots$$

$$b_n = \frac{1}{\pi}\int_0^{2\pi} v_0 \sin n\omega t\, d(\omega t) = \frac{2}{\pi}\int_0^{\pi} V_m \sin \omega t \sin n\omega t\, d(\omega t) - 0$$

Substituting the values of a_n and b_n, the expression for the output voltage is

$$v_0(t) = \frac{2V_m}{\pi} - \frac{4V_m}{3\pi}\cos 2\omega t - \frac{4V_m}{15\pi}\cos 4\omega t - \frac{4V_m}{35\pi}\cos 6\omega t - \cdots \tag{3.22}$$

Note: The output of a full-wave rectifier contains only even harmonics and the second harmonic is the most dominant one and its frequency is $2f(= 120$ Hz). The output voltage in Eq. (3.22) can be derived by spectrum multiplication of switching function, and this is explained in Appendix C.

Example 3.6 Finding the Input Power Factor of a Full-Wave Rectifier

A single-phase bridge rectifier that supplies a very high inductive load such as a dc motor is shown in Figure 3.7a. The turns ratio of the transformer is unity. The load is such that the motor draws a ripple-free armature current of I_a as shown in Figure 3.7b. Determine (a) the HF of input current, and (b) the input PF of the rectifier.

Solution

Normally, a dc motor is highly inductive and acts like a filter in reducing the ripple current of the load.

a. The waveforms for the input current and input voltage of the rectifier are shown in Figure 3.7b. The input current can be expressed in a Fourier series as

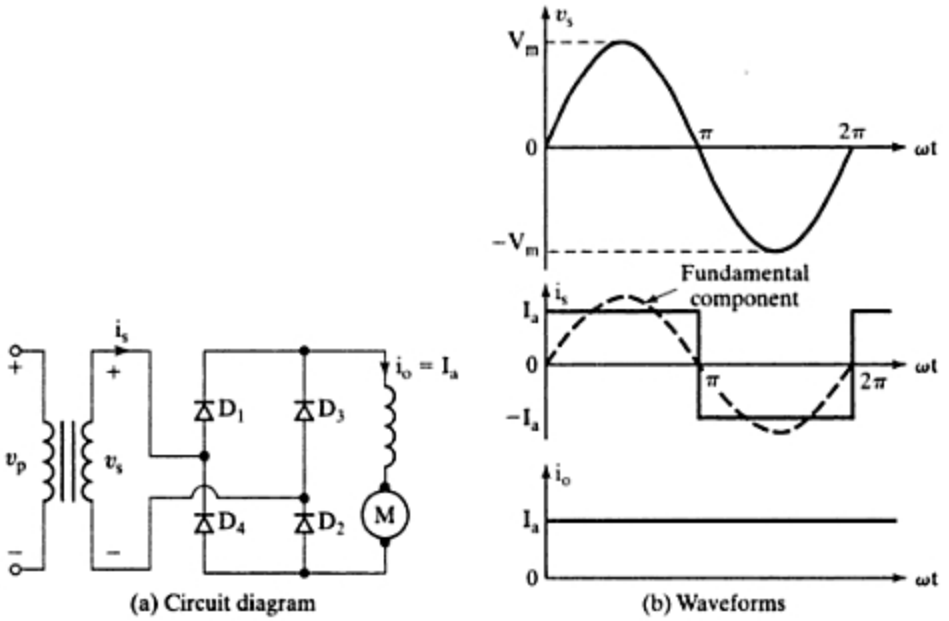
$$i_s(t) = I_{dc} + \sum_{n=1,3,\ldots}^{\infty} (a_n \cos n\omega t + b_n \sin n\omega t)$$

where

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} i_s(t)\, d(\omega t) = \frac{1}{2\pi}\int_0^{2\pi} I_a\, d(\omega t) = 0$$

$$a_n = \frac{1}{\pi}\int_0^{2\pi} i_s(t) \cos n\omega t\, d(\omega t) = \frac{2}{\pi}\int_0^{\pi} I_a \cos n\omega t\, d(\omega t) = 0$$

$$b_n = \frac{1}{\pi}\int_0^{2\pi} i_s(t) \sin n\omega t\, d(\omega t) = \frac{2}{\pi}\int_0^{\pi} I_a \sin n\omega t\, d(\omega t) = \frac{4I_a}{n\pi}$$



(a) Circuit diagram (b) Waveforms

FIGURE 3.7
Full-wave bridge rectifier with dc motor load.

Substituting the values of a_n and b_n, the expression for the input current is

$$i_s(t) = \frac{4I_a}{\pi}\left(\frac{\sin \omega t}{1} + \frac{\sin 3\omega t}{3} + \frac{\sin 5\omega t}{5} + \cdots\right) \tag{3.23}$$

The rms value of the fundamental component of input current is

$$I_{s1} = \frac{4I_a}{\pi\sqrt{2}} = 0.90I_a$$

The rms value of the input current is

$$I_s = \frac{4}{\pi\sqrt{2}} I_a\left[1 + \left(\frac{1}{3}\right)^2 + \left(\frac{1}{5}\right)^2 + \left(\frac{1}{7}\right)^2 + \left(\frac{1}{9}\right)^2 + \cdots\right]^{1/2} = I_a$$

From Eq. (3.10),

$$\text{HF} = \text{THD} = \left[\left(\frac{1}{0.90}\right)^2 - 1\right]^{1/2} = 0.4843 \quad \text{or} \quad 48.43\%$$

b. The displacement angle $\phi = 0$ and $\text{DF} = \cos\phi = 1$. From Eq. (3.11), the $\text{PF} = (I_{s1}/I_s)\cos\phi = 0.90$ (lagging).

Key Points of Section 3.4

- There are two types of single-phase rectifiers: center-tapped transformer and bridge. Their performances are almost identical, except the secondary current of

the center-tapped transformer carries unidirectional (dc) current and it requires larger VA rating. The center-tapped type is used in applications less than 100 W and the bridge rectifier is used in applications ranging from 100 W to 100 kW. The output voltage of the rectifiers contains harmonics whose frequencies are multiples of $2f$ (2 times the supply frequency).

3.5 SINGLE-PHASE FULL-WAVE RECTIFIER WITH *RL* LOAD

With a resistive load, the load current is identical in shape to the output voltage. In practice, most loads are inductive to a certain extent and the load current depends on the values of load resistance R and load inductance L. This is shown in Figure 3.8a. A battery of voltage E is added to develop generalized equations. If $v_s = V_m \sin \omega t = \sqrt{2}\, V_s \sin \omega t$ is the input voltage, the load current i_0 can be found from

$$L\frac{di_0}{dt} + Ri_0 + E = \sqrt{2}\, V_s \sin \omega t \quad \text{for} \quad i_0 \geq 0$$

which has a solution of the form

$$i_0 = \frac{\sqrt{2}V_s}{Z}\sin(\omega t - \theta) + A_1 e^{-(R/L)t} - \frac{E}{R} \tag{3.24}$$

where load impedance $Z = [R^2 + (\omega L)^2]^{1/2}$, load impedance angle $\theta = \tan^{-1}(\omega L/R)$, and V_s is the rms value of the input voltage.

Case 1: continuous load current. This is shown in Figure 3.8b. The constant A_1 in Eq. (3.24) can be determined from the condition: at $\omega t = \pi$, $i_0 = I_0$.

$$A_1 = \left(I_0 + \frac{E}{R} - \frac{\sqrt{2}V_s}{Z}\sin\theta\right)e^{(R/L)(\pi/\omega)}$$

Substitution of A_1 in Eq. (3.24) yields

$$i_0 = \frac{\sqrt{2}V_s}{Z}\sin(\omega t - \theta) + \left(I_0 + \frac{E}{R} - \frac{\sqrt{2}V_s}{Z}\sin\theta\right)e^{(R/L)(\pi/\omega - t)} - \frac{E}{R} \tag{3.25}$$

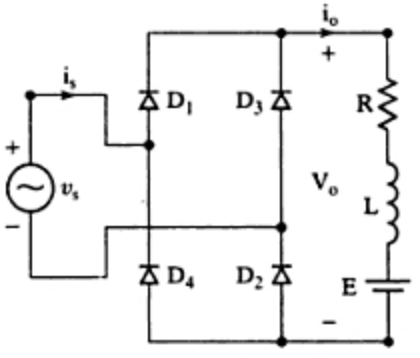
Under a steady-state condition, $i_0(\omega t = 0) = i_0(\omega t = \pi)$. That is, $i_0(\omega t = 0) = I_0$. Applying this condition, we get the value of I_0 as

$$I_0 = \frac{\sqrt{2}V_s}{Z}\sin\theta\,\frac{1 + e^{-(R/L)(\pi/\omega)}}{1 - e^{-(R/L)(\pi/\omega)}} - \frac{E}{R} \qquad \text{for } I_0 \geq 0 \tag{3.26}$$

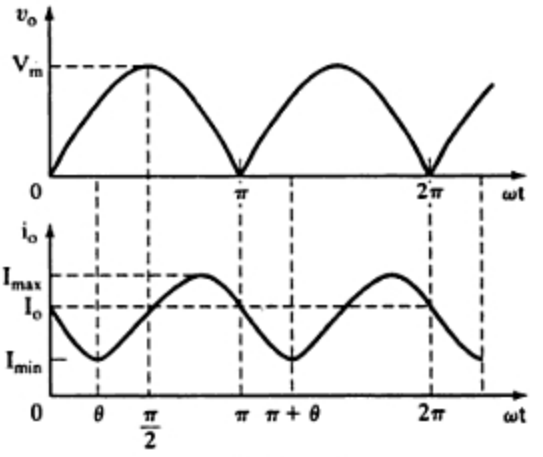
which, after substituting I_0 in Eq. (3.25) and simplification, gives

$$i_0 = \frac{\sqrt{2}V_s}{Z}\left[\sin(\omega t - \theta) + \frac{2}{1 - e^{-(R/L)(\pi/\omega)}}\sin\theta\, e^{-(R/L)t}\right] - \frac{E}{R}$$

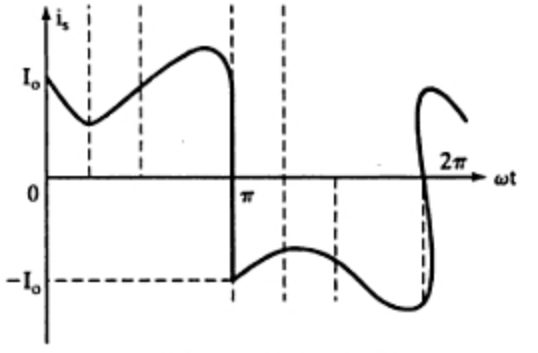
$$\text{for } 0 \leq (\omega t - \theta) \leq \pi \text{ and } i_0 \geq 0 \tag{3.27}$$



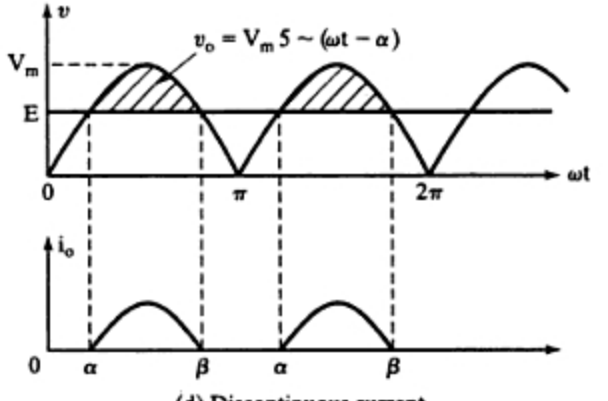
(a) Circuit



(b) Waveforms



(c) Supply line current



(d) Discontinuous current

FIGURE 3.8

Full-bridge rectifier with *RL* load.

The rms diode current can be found from Eq. (3.27) as

$$I_r = \left[\frac{1}{2\pi}\int_0^{\pi} i_0^2\, d(\omega t)\right]^{1/2}$$

and the rms output current can then be determined by combining the rms current of each diode as

$$I_{\text{rms}} = (I_r^2 + I_r^2)^{1/2} = \sqrt{2}I_r$$

The average diode current can also be found from Eq. (3.27) as

$$I_d = \frac{1}{2\pi}\int_0^{\pi} i_0\, d(\omega t)$$

Case 2: discontinuous load current. This is shown in Figure 3.8d. The load current flows only during the period $\alpha \le \omega t \le \beta$. Let us define $x = E/V_m = E/\sqrt{2}V_s$ as the load battery (*emf*) constant, called the *voltage ratio*. The diodes start to conduct at $\omega t = \alpha$ given by

$$\alpha = \sin^{-1}\frac{E}{V_m} = \sin^{-1}(x)$$

At $\omega t = \alpha$, $i_0(\omega t) = 0$ and Eq. (3.24) gives

$$A_1 = \left[\frac{E}{R} - \frac{\sqrt{2}V_s}{Z}\sin(\alpha - \theta)\right]e^{(R/L)(\alpha/\omega)}$$

which, after substituting in Eq. (3.24), yields the load current

$$i_0 = \frac{\sqrt{2}V_s}{Z}\sin(\omega t - \theta) + \left[\frac{E}{R} - \frac{\sqrt{2}V_s}{Z}\sin(\alpha - \theta)\right]e^{(R/L)(\alpha/\omega - t)} - \frac{E}{R} \qquad (3.28)$$

At $\omega t = \beta$, the current falls to zero, and $i_0(\omega t = \beta) = 0$. That is,

$$\frac{\sqrt{2}V_s}{Z}\sin(\beta - \theta) + \left[\frac{E}{R} - \frac{\sqrt{2}V_s}{Z}\sin(\alpha - \theta)\right]e^{(R/L)(\alpha-\beta)/\omega} - \frac{E}{R} = 0 \qquad (3.29)$$

Dividing Eq. (3.29) by $\sqrt{2}V_s/Z$, and substituting $R/Z = \cos\theta$ and $\omega L/R = \tan\theta$, we get

$$\sin(\beta - \theta) + \left(\frac{x}{\cos(\theta)} - \sin(\alpha - \theta)\right)e^{\frac{(\alpha-\beta)}{\tan(\theta)}} - \frac{x}{\cos(\theta)} = 0 \qquad (3.30)$$

β can be determined from this transcendental equation by an iterative (trial and error) method of solution. Start with $\beta = 0$, and increase its value by a very small amount until the left-hand side of this equation becomes zero.

As an example, Mathcad was used to find the value of β for $\theta = 30°, 60°$, and $x = 0$ to 1. The results are shown in Table 3.1. As k increases, β decreases. At $k = 1.0$, the diodes do not conduct and no current flows.

TABLE 3.1 Variations of Angle β with the Voltage Ratio, x

Voltage Ratio, x	0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
β for $\theta = 30°$	210	203	197	190	183	175	167	158	147	132	90
β for $\theta = 60°$	244	234	225	215	205	194	183	171	157	138	90

The rms diode current can be found from Eq. (3.28) as

$$I_r = \left[\frac{1}{2\pi}\int_{\alpha}^{\beta} i_0^2\, d(\omega t)\right]^{1/2}$$

The average diode current can also be found from Eq. (3.28) as

$$I_d = \frac{1}{2\pi}\int_{\alpha}^{\beta} i_0\, d(\omega t)$$

Boundary conditions: The condition for the discontinuous current can be found by setting I_0 in Eq. (3.26) to zero.

$$0 = \frac{V_s\sqrt{2}}{Z}\sin(\theta)\left[\frac{1 + e^{-(\frac{R}{L})(\frac{\pi}{\omega})}}{1 - e^{-(\frac{R}{L})(\frac{\pi}{\omega})}}\right] - \frac{E}{R}$$

which can be solved for the voltage ratio $x = E/(\sqrt{2}V_s)$ as

$$x(\theta): = \left[\frac{1 + e^{-(\frac{\pi}{\tan(\theta)})}}{1 - e^{-(\frac{\pi}{\tan(\theta)})}}\right]\sin(\theta)\cos(\theta) \tag{3.31}$$

The plot of the voltage ratio x against the load impedance angle θ is shown in Figure 3.9. The load angle θ cannot exceed π/2. The value of x is 63.67% at $\theta = 1.5567$ rad, 43.65% at $\theta = 0.52308$ rad (30°) and 0% at $\theta = 0$.

Example 3.7 Finding the Performance Parameters of a Full-Wave Rectifier with an *RL* Load

The single-phase full-wave rectifier of Figure 3.8a has $L = 6.5$ mH, $R = 2.5\ \Omega$, and $E = 10$ V. The input voltage is $V_s = 120$ V at 60 Hz. (a) Determine (1) the steady-state load current I_0 at $\omega t = 0$, (2) the average diode current I_d, (3) the rms diode current I_r, and (4) the rms output current I_{rms}. (b) Use PSpice to plot the instantaneous output current i_0. Assume diode parameters IS = 2.22E − 15, BV = 1800 V.

Solution

It is not known whether the load current is continuous or discontinuous. Assume that the load current is continuous and proceed with the solution. If the assumption is not correct, the load current is zero and then moves to the case for a discontinuous current.

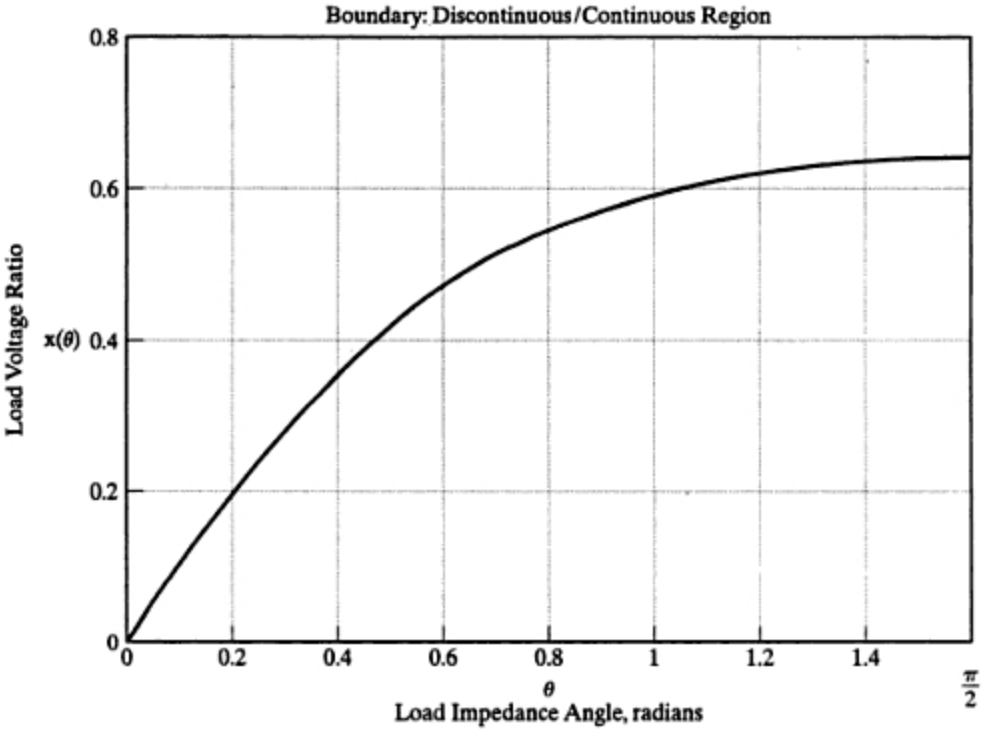


FIGURE 3.9

Boundary of continuous and discontinuous regions for single-phase rectifier.

a. $R = 2.5\ \Omega$, $L = 6.5$ mH, $f = 60$ Hz, $\omega = 2\pi \times 60 = 377$ rad/s, $V_s = 120$ V, $Z = [R^2 + (\omega L)^2]^{1/2} = 3.5\ \Omega$, and $\theta = \tan^{-1}(\omega L/R) = 44.43°$.

(1) The steady-state load current at $\omega t = 0$, $I_0 = 32.8$ A. Because $I_0 > 0$, the load current is continuous and the assumption is correct.

(2) The numerical integration of i_0 in Eq. (3.27) yields the average diode current as $I_d = 19.61$ A.

(3) By numerical integration of i_0^2 between the limits $\omega t = 0$ and π, we get the rms diode current as $I_r = 28.5$ A.

(4) The rms output current $I_{rms} = \sqrt{2} I_r = \sqrt{2} \times 28.50 = 40.3$ A.

Notes

1. i_0 has a minimum value of 25.2 A at $\omega t = 25.5°$ and a maximum value of 51.46 A at $\omega t = 125.25°$. i_0 becomes 27.41 A at $\omega t = \theta$ and 48.2 A at $\omega t = \theta + \pi$. Therefore, the minimum value of i_0 occurs approximately at $\omega t = \theta$.
2. The switching action of diodes makes the equations for currents nonlinear. A numerical method of solution for the diode currents is more efficient than the classical techniques. A Mathcad program is used to solve for I_0, I_d, and I_r by using numerical integration. Students are encouraged to verify the results of this example and to appreciate the usefulness of numerical solution, especially in solving nonlinear equations of diode circuits.

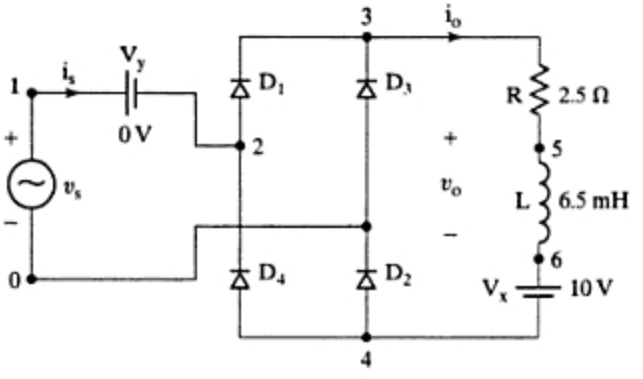


FIGURE 3.10
Single-phase bridge rectifier for PSpice simulation.

b. The single-phase bridge rectifier for PSpice simulation is shown in Figure 3.10. The list of the circuit file is as follows:

```
Example 3.7 Single-Phase Bridge Rectifier with RL load
VS     1     0     SIN (0   169.7V      60HZ)
L      5     6     6.5MH
R      3     5     2.5
VX     6     4     DC   10V ; Voltage source to measure the output current
D1     2     3     DMOD                      ; Diode model
D2     4     0     DMOD
D3     0     3     DMOD
D4     4     2     DMOD
VY     1           2     0DC
.MODEL    DMOD   D(IS=2.22E-15    BV=1800V)   ; Diode model parameters
.TRAN     1US    32MS     16.667MS            ; Transient analysis
.PROBE                                       ; Graphics postprocessor
.END
```

The PSpice plot of instantaneous output current i_0 is shown in Figure 3.11, which gives $I_0 = 31.83$ A, compared with the expected value of 32.8 A. A Dbreak diode was used in PSpice simulation to specify the diode parameters.

Key Points of Section 3.5

- An inductive load can make the load current continuous. There is a critical value of the load impedance angle θ for a given value of the load *emf* constant x to keep the load current continuous.

3.6 MULTIPHASE STAR RECTIFIERS

We have seen in Eq. (3.21) the average output voltage that could be obtained from single-phase full-wave rectifiers is $0.6366V_m$ and these rectifiers are used in applications up to a power level of 15 kW. For larger power output, *three-phase* and *multiphase* rectifiers are

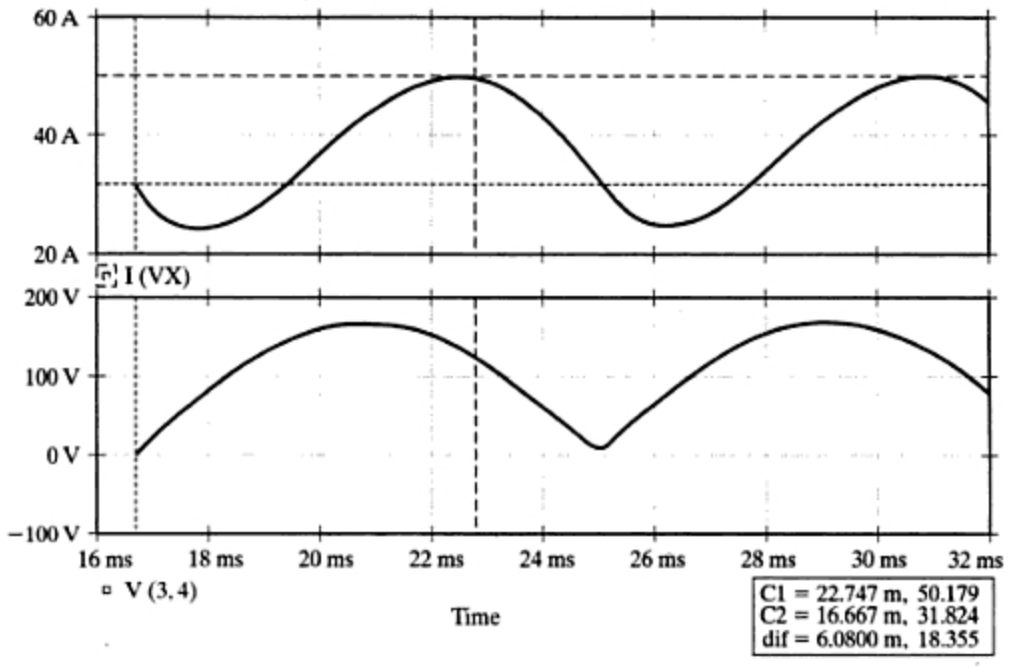


FIGURE 3.11

PSpice plot for Example 3.7.

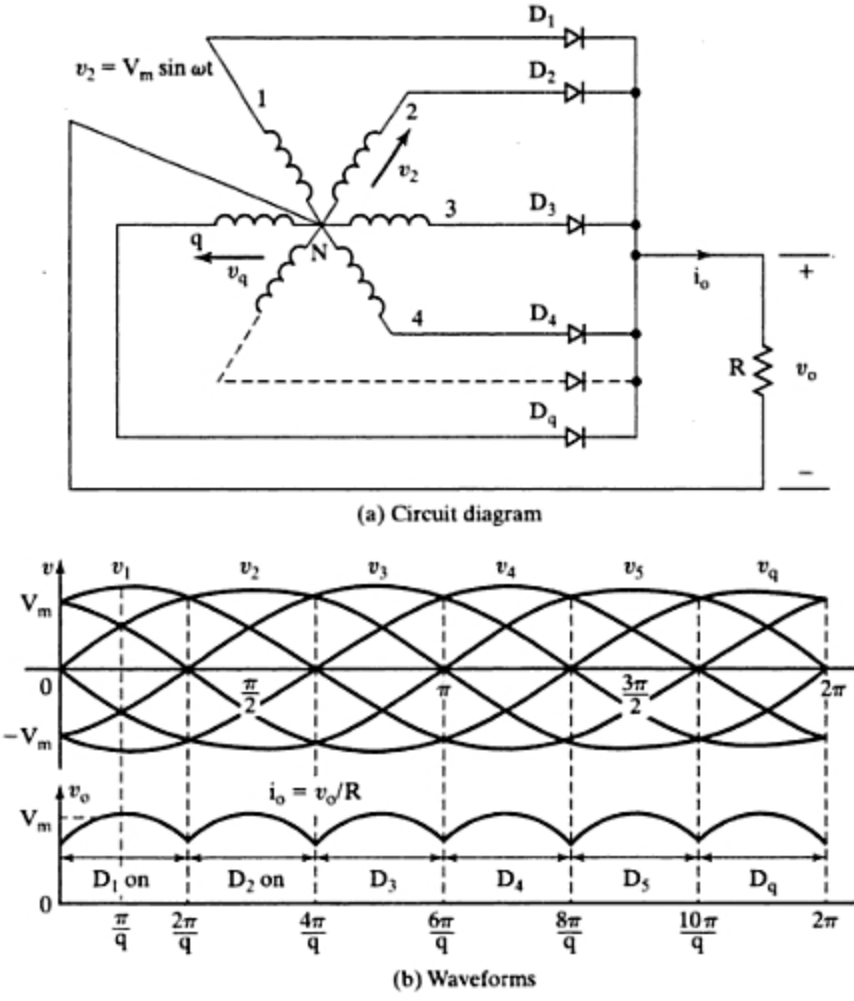
used. The Fourier series of the output voltage given by Eq. (3.22) indicates that the output contains harmonics and the frequency of the *fundamental component* is two times the source frequency ($2f$). In practice, a filter is normally used to reduce the level of harmonics in the load; and the size of the filter decreases with the increase in frequency of the harmonics. In addition to the larger power output of multiphase rectifiers, the fundamental frequency of the harmonics is also increased and is q times the source frequency (qf). This rectifier is also known as a star rectifier.

The rectifier circuit of Figure 3.5a can be extended to multiple phases by having multiphase windings on the transformer secondary as shown in Figure 3.12a. This circuit may be considered as q single-phase half-wave rectifiers and can be considered as a half-wave type. The kth diode conducts during the period when the voltage of kth phase is higher than that of other phases. The waveforms for the voltages and currents are shown in Figure 3.12b. The conduction period of each diode is $2\pi/q$.

It can be noticed from Figure 3.12b that the current flowing through the secondary winding is unidirectional and contains a dc component. Only one secondary winding carries current at a particular time, and as a result the primary must be connected in delta to eliminate the dc component in the input side of the transformer. This minimizes the harmonic content of the primary line current.

Assuming a cosine wave from π/q to $2\pi/q$, the average output voltage for a q-phase rectifier is given by

$$V_{dc} = \frac{2}{2\pi/q}\int_0^{\pi/q} V_m \cos \omega t \, d(\omega t) = V_m \frac{q}{\pi} \sin\frac{\pi}{q} \tag{3.32}$$



(a) Circuit diagram

(b) Waveforms

FIGURE 3.12

Multiphase rectifiers.

$$V_{\text{rms}} = \left[\frac{2}{2\pi/q}\int_0^{\pi/q} V_m^2 \cos^2 \omega t \, d(\omega t)\right]^{1/2}$$
$$= V_m\left[\frac{q}{2\pi}\left(\frac{\pi}{q} + \frac{1}{2}\sin\frac{2\pi}{q}\right)\right]^{1/2} \tag{3.33}$$

If the load is purely resistive, the peak current through a diode is $I_m = V_m/R$ and we can find the rms value of a diode current (or transformer secondary current) as

$$I_s = \left[\frac{2}{2\pi}\int_0^{\pi/q} I_m^2 \cos^2 \omega t \, d(\omega t)\right]^{1/2}$$
$$= I_m\left[\frac{1}{2\pi}\left(\frac{\pi}{q} + \frac{1}{2}\sin\frac{2\pi}{q}\right)\right]^{1/2} = \frac{V_{\text{rms}}}{R} \tag{3.34}$$

Example 3.8 Finding the Performance Parameters of a Three-Phase Star Rectifier

A three-phase star rectifier has a purely resistive load with R ohms. Determine (a) the efficiency, (b) the FF, (c) the RF, (d) the TUF factor, (e) the PIV of each diode, and (f) the peak current through a diode if the rectifier delivers $I_{dc} = 30$ A at an output voltage of $V_{dc} = 140$ V.

Solution

For a three-phase rectifier $q = 3$ in Eqs. (3.32) to (3.34)

a. From Eq. (3.32), $V_{dc} = 0.827V_m$ and $I_{dc} = 0.827V_m/R$. From Eq. (3.33), $V_{rms} = 0.84068V_m$ and $I_{rms} = 0.84068V_m/R$. From Eq. (3.1), $P_{dc} = (0.827V_m)^2/R$; from Eq. (3.2), $P_{ac} = (0.84068V_m)^2/R$; and from Eq. (3.3), the efficiency

$$\eta = \frac{(0.827V_m)^2}{(0.84068V_m)^2} = 96.77\%$$

b. From Eq. (3.5), the FF = 0.84068/0.827 = 1.0165 or 101.65%.

c. From Eq. (3.7), the RF = $\sqrt{1.0165^2 - 1} = 0.1824 = 18.24\%$.

d. The rms voltage of the transformer secondary, $V_s = V_m/\sqrt{2} = 0.707V_m$. From Eq. (3.34), the rms current of the transformer secondary,

$$I_s = 0.4854I_m = \frac{0.4854V_m}{R}$$

The VA rating of the transformer for $q = 3$ is

$$\text{VA} = 3V_sI_s = 3 \times 0.707V_m \times \frac{0.4854V_m}{R}$$

From Eq. (3.8),

$$\text{TUF} = \frac{0.827^2}{3 \times 0.707 \times 0.4854} = 0.6643$$

$$\text{PF} = \frac{0.84068^2}{3 \times 0.707 \times 0.4854} = 0.6844$$

e. The peak inverse voltage of each diode is equal to the peak value of the secondary line-to-line voltage. Three-phase circuits are reviewed in Appendix A. The line-to-line voltage is $\sqrt{3}$ times the phase voltage and thus PIV = $\sqrt{3}\,V_m$.

f. The average current through each diode is

$$I_d = \frac{2}{2\pi}\int_0^{\pi/q} I_m \cos \omega t \, d(\omega t) = I_m \frac{1}{\pi} \sin\frac{\pi}{q} \tag{3.35}$$

For $q = 3$, $I_d = 0.2757I_m$. The average current through each diode is $I_d = 30/3 = 10$ A and this gives the peak current as $I_m = 10/0.2757 = 36.27$ A.

Example 3.9 Finding the Fourier Series of a q-Phase Rectifier

a. Express the output voltage of a q-phase rectifier in Figure 3.12a in Fourier series.

b. If $q = 6$, $V_m = 170$ V, and the supply frequency is $f = 60$ Hz, determine the rms value of the dominant harmonic and its frequency.

Solution

a. The waveforms for q-pulses are shown in Figure 3.12b and the frequency of the output is q times the fundamental component (qf). To find the constants of the Fourier series, we integrate from $-\pi/q$ to π/q and the constants are

$$b_n = 0$$

$$a_n = \frac{1}{\pi/q}\int_{-\pi/q}^{\pi/q} V_m \cos \omega t \cos n\omega t \, d(\omega t)$$

$$= \frac{qV_m}{\pi}\left\{\frac{\sin[(n-1)\pi/q]}{n-1} + \frac{\sin[(n+1)\pi/q]}{n+1}\right\}$$

$$= \frac{qV_m}{\pi}\frac{(n+1)\sin[(n-1)\pi/q] + (n-1)\sin[(n+1)\pi/q]}{n^2-1}$$

After simplification and then using trigonometric relationships, we get

$$\sin(A + B) = \sin A \cos B + \cos A \sin B$$

and

$$\sin(A - B) = \sin A \cos B - \cos A \sin B$$

we get

$$a_n = \frac{2qV_m}{\pi(n^2-1)}\left(n \sin\frac{n\pi}{q}\cos\frac{\pi}{q} - \cos\frac{n\pi}{q}\sin\frac{\pi}{q}\right) \tag{3.36}$$

For a rectifier with q pulses per cycle, the harmonics of the output voltage are: qth, $2q$th, $3q$th, and $4q$th, and Eq. (3.36) is valid for $n = 0, 1q, 2q, 3q$. The term $\sin(n\pi/q) = \sin\pi = 0$ and Eq. (3.36) becomes

$$a_n = \frac{-2qV_m}{\pi(n^2-1)}\left(\cos\frac{n\pi}{q}\sin\frac{\pi}{q}\right)$$

The dc component is found by letting $n = 0$ and is

$$V_{dc} = \frac{a_0}{2} = V_m\frac{q}{\pi}\sin\frac{\pi}{q} \tag{3.37}$$

which is the same as Eq. (3.32). The Fourier series of the output voltage v_0 is expressed as

$$v_0(t) = \frac{a_0}{2} + \sum_{n=q,2q,\ldots}^{\infty} a_n \cos n\omega t$$

Substituting the value of a_n, we obtain

$$v_0 = V_m \frac{q}{\pi} \sin\frac{\pi}{q}\left(1 - \sum_{n=q,2q,\ldots}^{\infty} \frac{2}{n^2-1}\cos\frac{n\pi}{q}\cos n\omega t\right) \tag{3.38}$$

b. For $q = 6$, the output voltage is expressed as

$$v_0(t) = 0.9549V_m\left(1 + \frac{2}{35}\cos 6\omega t - \frac{2}{143}\cos 12\omega t + \cdots\right) \tag{3.39}$$

The sixth harmonic is the dominant one. The rms value of a sinusoidal voltage is $1/\sqrt{2}$ times its peak magnitude, and the rms of the sixth harmonic is $V_{6h} = 0.9549V_m \times 2/(35 \times \sqrt{2}) = 6.56$ V and its frequency is $f_6 = 6f = 360$ Hz.

Key Points of Section 3.6

- A multiphase rectifier increases the amount of dc component and lowers the amount of the harmonic components. The output voltage of a p-phase rectifier contains harmonics whose frequencies are multiples of p (p times the supply frequency), *pf*.

3.7 THREE-PHASE BRIDGE RECTIFIERS

A three-phase bridge rectifier is commonly used in high-power applications and it is shown in Figure 3.13. This is a *full-wave rectifier*. It can operate with or without a transformer and gives six-pulse ripples on the output voltage. The diodes are numbered in order of conduction sequences and each one conducts for 120°. The conduction sequence for diodes is $D_1 - D_2$, $D_3 - D_2$, $D_3 - D_4$, $D_5 - D_4$, $D_5 - D_6$, and $D_1 - D_6$. The pair of diodes which are connected between that pair of supply lines having the highest amount of instantaneous line-to-line voltage will conduct. The line-to-line voltage is $\sqrt{3}$ times the phase voltage of a three-phase Y-connected source. The waveforms and conduction times of diodes are shown in Figure 3.14 [4].

If V_m is the peak value of the phase voltage, then the instantaneous phase voltages can be described by

$$v_{an} = V_m \sin(\omega t) \quad v_{bn} = V_m \sin(\omega t - 120°) \quad v_{cn} = V_m \sin(\omega t - 240°)$$

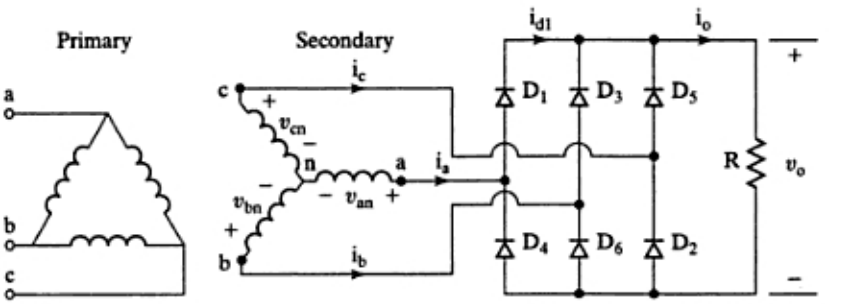


FIGURE 3.13
Three-phase bridge rectifier.

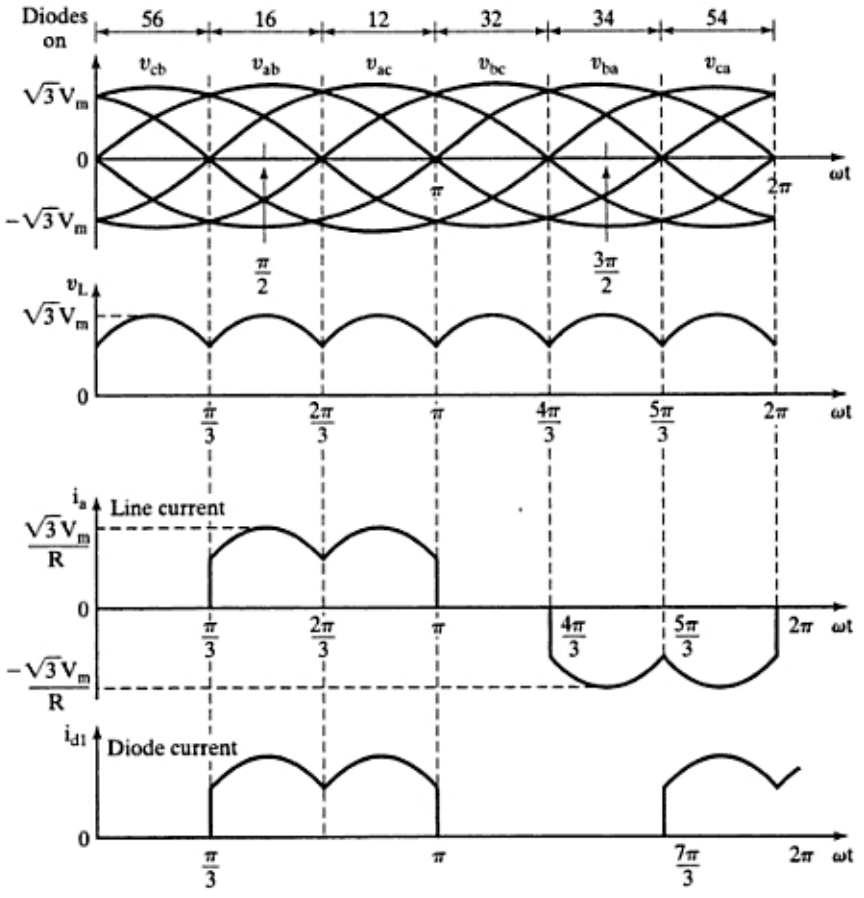


FIGURE 3.14

Waveforms and conduction times of diodes.

Because the line–line voltage leads the phase voltage by 30°, the instantaneous line–line voltages can be described by

$$v_{ab} = \sqrt{3}\,V_m \sin(\omega t + 30°) \quad v_{bc} = \sqrt{3}\,V_m \sin(\omega t - 90°)$$
$$v_{ca} = \sqrt{3}\,V_m \sin(\omega t - 210°)$$

The average output voltage is found from

$$V_{dc} = \frac{2}{2\pi/6}\int_0^{\pi/6} \sqrt{3}\,V_m \cos \omega t\, d(\omega t)$$

$$= \frac{3\sqrt{3}}{\pi} V_m = 1.654 V_m \tag{3.40}$$

where V_m is the peak phase voltage. The rms output voltage is

$$V_{rms} = \left[\frac{2}{2\pi/6}\int_0^{\pi/6} 3V_m^2 \cos^2 \omega t \, d(\omega t)\right]^{1/2}$$

$$= \left(\frac{3}{2} + \frac{9\sqrt{3}}{4\pi}\right)^{1/2} V_m = 1.6554V_m \tag{3.41}$$

If the load is purely resistive, the peak current through a diode is $I_m = \sqrt{3}\, V_m/R$ and the rms value of the diode current is

$$I_r = \left[\frac{4}{2\pi}\int_0^{\pi/6} I_m^2 \cos^2 \omega t \, d(\omega t)\right]^{1/2}$$

$$= I_m\left[\frac{1}{\pi}\left(\frac{\pi}{6} + \frac{1}{2}\sin\frac{2\pi}{6}\right)\right]^{1/2}$$

$$= 0.5518I_m \tag{3.42}$$

and the rms value of the transformer secondary current,

$$I_s = \left[\frac{8}{2\pi}\int_0^{\pi/6} I_m^2 \cos^2 \omega t \, d(\omega t)\right]^{1/2}$$

$$= I_m\left[\frac{2}{\pi}\left(\frac{\pi}{6} + \frac{1}{2}\sin\frac{2\pi}{6}\right)\right]^{1/2}$$

$$= 0.7804I_m \tag{3.43}$$

where I_m is the peak secondary line current.

For a three-phase rectifier $q = 6$, Eq. (3.38) gives the instantaneous output voltage as

$$v_0(t) = 0.9549V_m\left(1 + \frac{2}{35}\cos(6\omega t) - \frac{2}{143}\cos(12\omega t) + \cdots\right) \tag{3.44}$$

Example 3.10 Finding the Performance Parameters of a Three-Phase Bridge Rectifier

A three-phase bridge rectifier has a purely resistive load of R. Determine (a) the efficiency, (b) the FF, (c) the RF, (d) the TUF, (e) the peak inverse (or reverse) voltage (PIV) of each diode, and (f) the peak current through a diode. The rectifier delivers $I_{dc} = 60$ A at an output voltage of $V_{dc} = 280.7$ V and the source frequency is 60 Hz.

Solution

a. From Eq. (3.40), $V_{dc} = 1.654V_m$ and $I_{dc} = 1.654V_m/R$. From Eq. (3.41), $V_{rms} = 1.6554V_m$ and $I_{rms} = 1.6554V_m/R$. From Eq. (3.1), $P_{dc} = (1.654V_m)^2/R$, from Eq. (3.2), $P_{ac} = (1.6554V_m)^2/R$, and from Eq. (3.3) the efficiency

$$\eta = \frac{(1.654V_m)^2}{(1.6554V_m)^2} = 99.83\%$$

b. From Eq. (3.5), the FF = 1.6554/1.654 = 1.0008 = 100.08%.

c. From Eq. (3.6), the RF = $\sqrt{1.0008^2 - 1} = 0.04 = 4\%$.

d. From Eq. (3.15), the rms voltage of the transformer secondary, $V_s = 0.707V_m$. From Eq. (3.43), the rms current of the transformer secondary,

$$I_s = 0.7804I_m = 0.7804 \times \sqrt{3}\,\frac{V_m}{R}$$

The VA rating of the transformer,

$$\text{VA} = 3V_sI_s = 3 \times 0.707V_m \times 0.7804 \times \sqrt{3}\,\frac{V_m}{R}$$

From Eq. (3.8),

$$\text{TUF} = \frac{1.654^2}{3 \times \sqrt{3} \times 0.707 \times 0.7804} = 0.9542$$

e. From Eq. (3.40), the peak line-to-neutral voltage is $V_m = 280.7/1.654 = 169.7$ V. The peak inverse voltage of each diode is equal to the peak value of the secondary line-to-line voltage, PIV = $\sqrt{3}\,V_m = \sqrt{3} \times 169.7 = 293.9$ V.

f. The average current through each diode is

$$I_d = \; = \frac{4}{2\pi}\int_0^{\pi/6} I_m \cos \omega t \, d(\omega t) = I_m \frac{2}{\pi} \sin \frac{\pi}{6} = 0.3183I_m$$

The average current through each diode is $I_d = 60/3 = 20$ A; therefore, the peak current is $I_m = 20/0.3183 = 62.83$ A.

Note: This rectifier has considerably improved performances compared with those of the multiphase rectifier in Figure 3.12 with six pulses.

Key Points of Section 3.6

- A three-phase bridge rectifier has considerably improved performances compared with those of single-phase rectifiers.

3.8 THREE-PHASE BRIDGE RECTIFIER WITH *RL* LOAD

Equations that are derived in Section 3.5 can be applied to determine the load current of a three-phase rectifier with an *RL* load (similar to Figure 3.15). It can be noted from Figure 3.14 that the output voltage becomes

$$v_{ab} = \sqrt{2}\,V_{ab} \sin \omega t \quad \text{for} \quad \frac{\pi}{3} \le \omega t \le \frac{2\pi}{3}$$

where V_{ab} is the line-to-line rms input voltage. The load current i_0 can be found from

$$L\frac{di_0}{dt} + Ri_0 + E = \sqrt{2}\,V_{ab} \sin \omega t$$

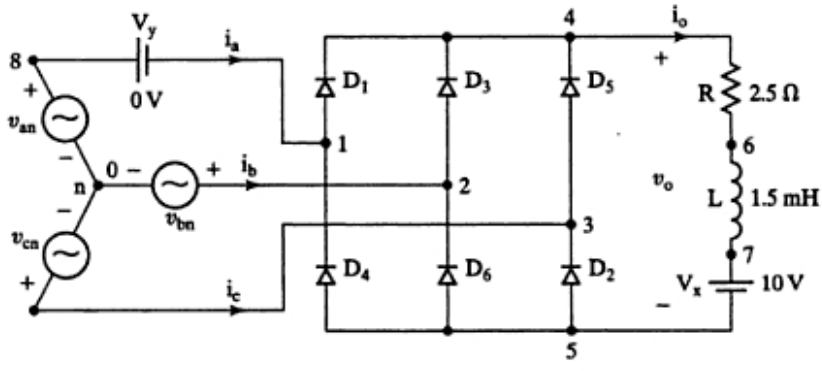


FIGURE 3.15

Three-phase bridge rectifier for PSpice simulation.

which has a solution of the form

$$i_0 = \frac{\sqrt{2}V_{ab}}{Z}\sin(\omega t - \theta) + A_1 e^{-(R/L)t} - \frac{E}{R} \tag{3.45}$$

where load impedance $Z = [R^2 + (\omega L)^2]^{1/2}$ and load impedance angle $\theta = \tan^{-1}(\omega L/R)$. The constant A_1 in Eq. (3.45) can be determined from the condition: at $\omega t = \pi/3$, $i_0 = I_0$.

$$A_1 = \left[I_0 + \frac{E}{R} - \frac{\sqrt{2}V_{ab}}{Z}\sin\left(\frac{\pi}{3} - \theta\right)\right]e^{(R/L)(\pi/3\omega)}$$

Substitution of A_1 in Eq. (3.45) yields

$$i_0 = \frac{\sqrt{2}V_{ab}}{Z}\sin(\omega t - \theta) + \left[I_0 + \frac{E}{R} - \frac{\sqrt{2}V_{ab}}{Z}\sin\left(\frac{\pi}{3} - \theta\right)\right]e^{(R/L)(\pi/3\omega - t)} - \frac{E}{R} \tag{3.46}$$

Under a steady-state condition, $i_0(\omega t = 2\pi/3) = i_0(\omega t = \pi/3)$. That is, $i_0(\omega t = 2\pi/3) = I_0$. Applying this condition, we get the value of I_0 as

$$I_0 = \frac{\sqrt{2}V_{ab}}{Z}\frac{\sin(2\pi/3 - \theta) - \sin(\pi/3 - \theta)e^{-(R/L)(\pi/3\omega)}}{1 - e^{-(R/L)(\pi/3\omega)}} - \frac{E}{R} \qquad \text{for } I_0 \geq 0 \tag{3.47}$$

which, after substitution in Eq. (3.46) and simplification, gives

$$i_0 = \frac{\sqrt{2}V_{ab}}{Z}\left[\sin(\omega t - \theta) + \frac{\sin(2\pi/3 - \theta) - \sin(\pi/3 - \theta)}{1 - e^{-(R/L)(\pi/3\omega - t)}}e^{(R/L)(\pi/3\omega - t)}\right] - \frac{E}{R} \quad \text{for } \pi/3 \leq \omega t \leq 2\pi/3 \text{ and } i_0 \geq 0 \tag{3.48}$$

The rms diode current can be found from Eq. (3.48) as

$$I_r = \left[\frac{2}{2\pi}\int_{\pi/3}^{2\pi/3} i_0^2\, d(\omega t)\right]^{1/2}$$

and the rms output current can then be determined by combining the rms current of each diode as

$$I_{\text{rms}} = (I_r^2 + I_r^2 + I_r^2)^{1/2} = \sqrt{3}\, I_r$$

The average diode current can also be found from Eq. (3.47) as

$$I_d = \frac{2}{2\pi}\int_{\pi/3}^{2\pi/3} i_0\, d(\omega t)$$

Boundary conditions: The condition for the discontinuous current can be found by setting I_0 in Eq. (3.47) to zero.

$$\frac{\sqrt{2}V_{AB}}{Z}\cdot\left[\frac{\sin\left(\frac{2\pi}{3}-\theta\right)-\sin\left(\frac{\pi}{3}-\theta\right)e^{-\left(\frac{R}{L}\right)\left(\frac{\pi}{\omega}\right)}}{1-e^{-\left(\frac{R}{L}\right)\left(\frac{\pi}{\omega}\right)}}\right]-\frac{E}{R}=0$$

which can be solved for the voltage ratio $x = E/(\sqrt{2}V_{AB})$ as

$$x(\theta) := \left[\frac{\sin\left(\frac{2\pi}{3}-\theta\right)-\sin\left(\frac{\pi}{3}-\theta\right)e^{-\left(\frac{\pi}{3\tan(\theta)}\right)}}{1-e^{-\left(\frac{\pi}{3\tan(\theta)}\right)}}\right]\cos(\theta) \qquad (3.49)$$

The plot of the voltage ratio x against the load impedance angle θ is shown in Figure 3.16. The load angle θ cannot exceed $\pi/2$. The value of x is 95.49% at $\theta = 1.5598$ rad, 95.03% at $\theta = 0.52308$ (30°), and 86.68% at $\theta = 0$.

Example 3.11 Finding the Performance Parameters of a Three-Phase Bridge Rectifier with an *RL* Load

The three-phase full-wave rectifier of Figure 3.15 has a load of $L = 1.5$ mH, $R = 2.5\ \Omega$, and $E = 10$ V. The line-to-line input voltage is $V_{ab} = 208$ V, 60 Hz. (a) Determine (1) the steady-state load current I_0 at $\omega_t = \pi/3$, (2) the average diode current I_0, (3) the rms diode current I_r, and (4) the rms output current I_{rms}. (b) Use PSpice to plot the instantaneous output current i_0. Assume diode parameters IS = 2.22E − 15, BV = 1800 V.

Solution

a. $R = 2.5\ \Omega$, $L = 1.5$ mH, $f = 60$ Hz, $\omega = 2\pi \times 60 = 377$ rad/s, $V_{ab} = 208$ V, $Z = [R^2 + (\omega L)^2]^{1/2} = 2.56\ \Omega$, and $\theta = \tan^{-1}(\omega L/R) = 12.74°$.

1. The steady-state load current at $\omega t = \pi/3$, $I_0 = 105.77$ A.
2. The numerical integration of i_0 in Eq. (3.48) yields the average diode current as $I_d = 36.09$ A. Because $I_0 > 0$, the load current is continuous.

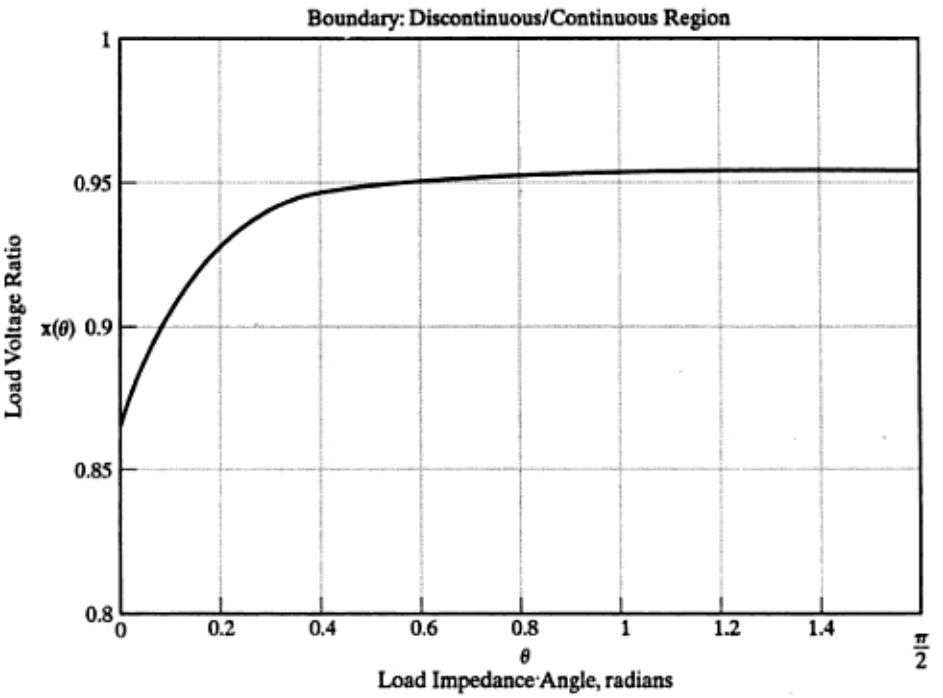


FIGURE 3.16

Boundary of continuous and discontinuous regions for three-phase rectifier.

3. By numerical integration of i_0^2 between the limits $\omega t = \pi/3$ and $2\pi/3$, we get the rms diode current as $I_r = 62.733$ A.
4. The rms output current $I_{rms} = \sqrt{3} I_r = \sqrt{3} \times 62.53 = 108.31$ A.

b. The three-phase bridge rectifier for PSpice simulation is shown in Figure 3.15. The list of the circuit file is as follows:

```
Example 3.11      Three-Phase Bridge Rectifier with RL load
VAN    8     0    SIN (0 169.7V 60HZ)
VBN    2     0    SIN (0 169.7V 60HZ 0 0 120DEG)
VCN    3     0    SIN (0 169.7V 60HZ 0 0 240DEG)
L      6     7    1.5MH
R      4     6    2.5
VX     7     5    DC 10V ; Voltage source to measure the output current
VY     8     1    DC  0V ; Voltage source to measure the input current
D1     1     4    DMOD                    ; Diode model
D3     2     4    DMOD
D5     3     4    DMOD
D2     5     3    DMOD
D4     5     1    DMOD
```

```
D6     5     2     DMOD
.MODEL     DMOD     D (IS=2.22E-15 BV=1800V)  ; Diode model parameters
.TRAN      10US     25MS     16.667MS  10US    ; Transient analysis
.PROBE                                         ; Graphics postprocessor
.options ITL5=0 abstol = 1.000n reltol = .01 vntol = 1.000m
.END
```

The PSpice plot of instantaneous output current i_0 is shown in Figure 3.17, which gives $I_0 = 104.89$ A, compared with the expected value of 105.77 A. A Dbreak diode was used in PSpice simulation to include the specified diode parameters.

Example 3.12 Finding the Input Power Factor of a Three-Phase Rectifier with a Highly Inductive Load

The load current of a three-phase rectifier in Figure 3.13 is continuous, with a negligible ripple content. Express the input current in Fourier series, and determine the HF of the input current, the DF, and the input PF.

Solution

The waveform of the line current is shown in Figure 3.14. The line current is symmetric at the angle ($q = p/6$) when the phase voltage becomes zero, not when the line–line voltage v_{ab}

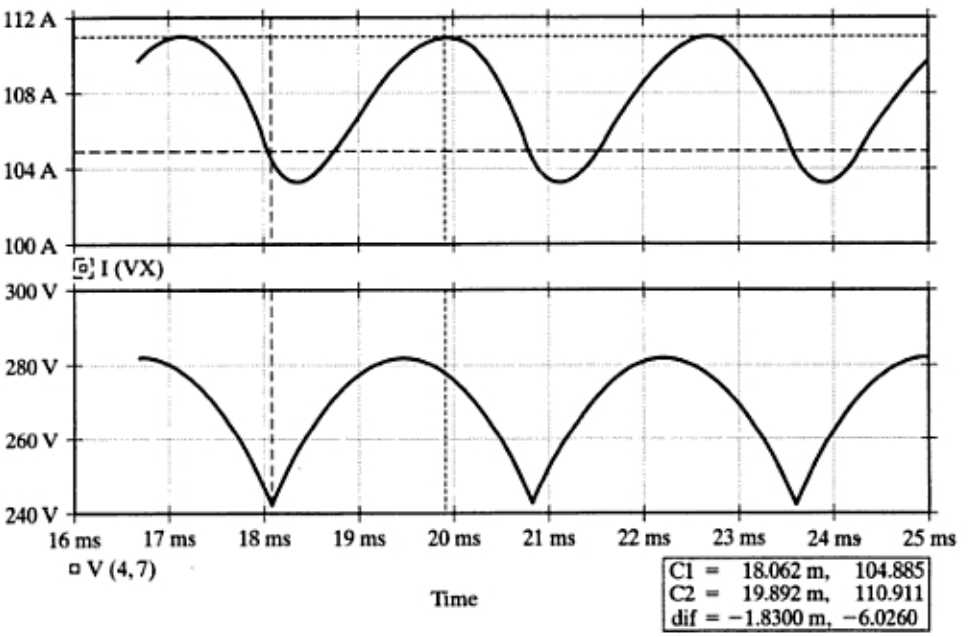


FIGURE 3.17

PSpice plot for Example 3.11.

becomes zero. Thus, for satisfying the condition of $f(x + 2\pi) = f(x)$, the input current can be described by

$$i_s(t) = I_a \quad \text{for} \quad \frac{\pi}{6} \le \omega t \le \frac{5\pi}{6}$$

$$i_s(t) = -I_a \quad \text{for} \quad \frac{7\pi}{6} \le \omega t \le \frac{11\pi}{6}$$

which can be expressed in a Fourier series as

$$i_s(t) = I_{dc} + \sum_{n=1}^{\infty} (a_n \cos(n\omega t) + b_n \sin(n\omega t)) = \sum_{n=1}^{\infty} c_n \sin(n\omega t + \phi_n)$$

where the coefficients are

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} i_s(t) \cdot d(\omega t) = \frac{1}{2\pi}\int_0^{2\pi} I_a \cdot d(\omega t) = 0$$

$$a_n = \frac{1}{\pi}\int_0^{2\pi} i_s(t) \cos(n\omega t)\, d(\omega t) = \frac{1}{\pi}\left[\int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} I_a \cos(n\omega t)\, d(\omega t) - \int_{\frac{7\pi}{6}}^{\frac{11\pi}{6}} I_a \cos(n\omega t)\, d(\omega t)\right] = 0$$

$$b_n = \frac{1}{\pi}\int_0^{2\pi} i_s(t) \cos(n\omega t)\, d(\omega t) = \frac{1}{\pi}\left[\int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} I_a \sin(n\omega t)\, d(\omega t) - \int_{\frac{7\pi}{6}}^{\frac{11\pi}{6}} I_a \sin(n\omega t)\, d(\omega t)\right]$$

which, after integration and simplification, gives b_n as

$$b_n = \frac{-4I_a}{n\pi}\cos(n\pi)\sin\left(\frac{n\pi}{2}\right)\sin\left(\frac{n\pi}{3}\right) \quad \text{for} \quad n = 1, 5, 7, 11, 13, \ldots$$

$$b_n = 0 \quad \text{for} \quad n = 2, 3, 4, 6, 8, 9, \ldots$$

$$c_n = \sqrt{(a_n)^2 + (b_n)^2} = \frac{-4I_a}{n\pi}\cos(n\pi)\sin\left(\frac{n\pi}{2}\right)\sin\left(\frac{n\pi}{3}\right)$$

$$\phi_n = \arctan\left(\frac{a_n}{b_n}\right) = 0$$

Thus, the Fourier series of the input current is given by

$$i_s = \sum_{n=1}^{\infty} \frac{4.\sqrt{3}I_a}{2\pi}\left(\frac{\sin(\omega t)}{1} - \frac{\sin(5\omega t)}{5} - \frac{\sin(7\omega t)}{7} + \frac{\sin(11\omega t)}{11} + \frac{\sin(13\omega t)}{13} - \frac{\sin(17\omega t)}{17} - \cdots\right) \tag{3.50}$$

The rms value of the nth harmonic input current is given by

$$I_{sn} = \frac{1}{\sqrt{2}}(a_n^2 + b_n^2)^{1/2} = \frac{2\sqrt{2}I_a}{n\pi}\sin\frac{n\pi}{3} \tag{3.51}$$

The rms value of the fundamental current is

$$I_{s1} = \frac{\sqrt{6}}{\pi}I_a = 0.7797I_a$$

The rms input current

$$I_s = \left[\frac{2}{2\pi}\int_{\pi/6}^{5\pi/6} I_a^2\, d(\omega t)\right]^{1/2} = I_a\sqrt{\frac{2}{3}} = 0.8165 I_a$$

$$\text{HF} = \left[\left(\frac{I_s}{I_{s1}}\right)^2 - 1\right]^{1/2} = \left[\left(\frac{\pi}{3}\right)^2 - 1\right]^{1/2} = 0.3108 \text{ or } 31.08\%$$

$$\text{DF} = \cos\phi_1 = \cos(0) = 1$$

$$\text{PF} = \frac{I_{s1}}{I_s}\cos(0) = \frac{0.7797}{0.8165} = 0.9549$$

Note: If we compare the PF with that of Example 3.10, where the load is purely resistive, we can notice that the input PF depends on the load angle. For a purely resistive load, PF = 0.8166.

Key Points of Section 3.8

- An inductive load can make the load current continuous. The critical value of the load electromotive force (emf) constant x for a given load impedance angle θ is higher than that of a single-phase rectifier; that is, $x = 86.68\%$ at $\theta = 0$.
- With a highly inductive load, the input current of a rectifier becomes an ac square wave. The input power factor of a three-phase rectifier is 0.955, which is higher than 0.9 for a single-phase rectifier.

3.9 COMPARISONS OF DIODE RECTIFIERS

The goal of a rectifier is to yield a dc output voltage at a given dc output power. Therefore, it is more convenient to express the performance parameters in terms of V_{dc} and P_{dc}. For example, the rating and turns ratio of the transformer in a rectifier circuit can easily be determined if the rms input voltage to the rectifier is in terms of the required output voltage V_{dc}. The important parameters are summarized in Table 3.2 [3]. Due to their relative merits, the single-phase and three-phase bridge rectifiers are commonly used.

Key Points of Section 3.9

- The single-phase and three-phase bridge rectifiers, which have relative merits, are commonly used for dc–ac conversion.

3.10 RECTIFIER CIRCUIT DESIGN

The design of a rectifier involves determining the ratings of semiconductor diodes. The ratings of diodes are normally specified in terms of average current, rms current, peak current, and peak inverse voltage. There are no standard procedures for the design, but it is required to determine the shapes of the diode currents and voltages.

We have noticed in Eqs. (3.20), (3.22), and (3.39) that the output of the rectifiers contain harmonics. Filters can be used to smooth out the dc output voltage of

TABLE 3.2 Performance Parameters of Diode Rectifiers with a Resistive Load

Performance Parameters	Single-Phase Rectifier with Center-Tapped Transformer	Single-Phase Bridge Rectifier	Six-Phase Star Rectifier	Three-Phase Bridge Rectifier
Peak repetitive reverse voltage, V_{RRM}	$3.14V_{dc}$	$1.57V_{dc}$	$2.09V_{dc}$	$1.05V_{dc}$
Rms input voltage per transformer leg, V_s	$1.11V_{dc}$	$1.11V_{dc}$	$0.74V_{dc}$	$0.428V_{dc}$
Diode average current, $I_{F(AV)}$	$0.50I_{dc}$	$0.50I_{dc}$	$0.167I_{dc}$	$0.333I_{dc}$
Peak repetitive forward current, I_{FRM}	$1.57I_{dc}$	$1.57I_{dc}$	$6.28I_{dc}$	$3.14I_{dc}$
Diode rms current, $I_{F(RMS)}$	$0.785I_{dc}$	$0.785I_{dc}$	$0.409I_{dc}$	$0.579I_{dc}$
Form factor of diode current, $I_{F(RMS)}/I_{F(AV)}$	1.57	1.57	2.45	1.74
Rectification ratio, η	0.81	0.81	0.998	0.998
Form factor, FF	1.11	1.11	1.0009	1.0009
Ripple factor, RF	0.482	0.482	0.042	0.042
Transformer rating primary, VA	$1.23P_{dc}$	$1.23P_{dc}$	$1.28P_{dc}$	$1.05P_{dc}$
Transformer rating secondary, VA	$1.75P_{dc}$	$1.23P_{dc}$	$1.81P_{dc}$	$1.05P_{dc}$
Output ripple frequency, f_r	$2f_s$	$2f_s$	$6f_s$	$6f_s$

the rectifier and these are known as *dc filters*. The dc filters are usually of *L*, *C*, and *LC* type, as shown in Figure 3.18. Due to rectification action, the input current of the rectifier contains harmonics also and an *ac filter* is used to filter out some of the harmonics from the supply system. The ac filter is normally of *LC* type, as shown in Figure 3.19.

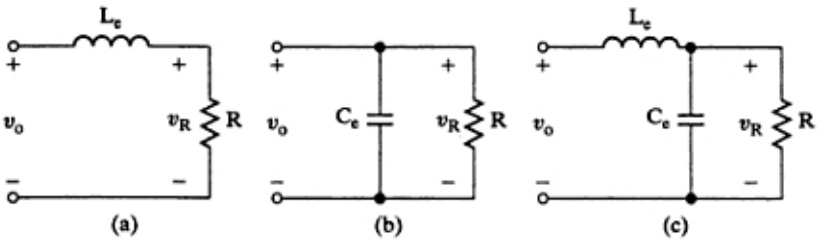


FIGURE 3.18
Dc filters.

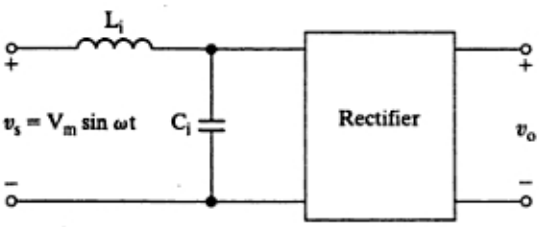


FIGURE 3.19
Ac filters.

Normally, the filter design requires determining the magnitudes and frequencies of the harmonics. The steps involved in designing rectifiers and filters are explained by examples.

Example 3.13 Finding the Diode Ratings from the Diode Currents

A three-phase bridge rectifier supplies a highly inductive load such that the average load current is $I_{dc} = 60$ A and the ripple content is negligible. Determine the ratings of the diodes if the line-to-neutral voltage of the Y-connected supply is 120 V at 60 Hz.

Solution

The currents through the diodes are shown in Figure 3.20. The average current of a diode $I_d = 60/3 = 20$ A. The rms current is

$$I_r = \left[\frac{1}{2\pi}\int_{\pi/3}^{\pi} I_{dc}^2\, d(\omega t)\right]^{1/2} = \frac{I_{dc}}{\sqrt{3}} = 34.64 \text{ A}$$

The PIV $= \sqrt{3}\, V_m = \sqrt{3} \times \sqrt{2} \times 120 = 294$ V.

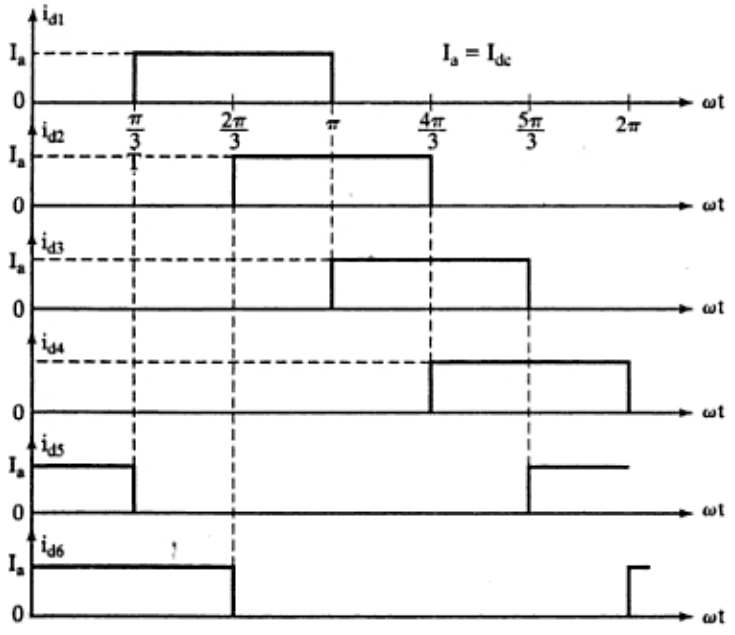


FIGURE 3.20
Current through diodes.

Note: The factor of $\sqrt{2}$ is used to convert rms to peak value.

Example 3.14 Finding the Diode Average and rms Currents from the Waveforms

The current through a diode is shown in Figure 3.21. Determine (a) the rms current, and (b) the average diode current if $t_1 = 100\ \mu s$, $t_2 = 350\ \mu s$, $t_3 = 500\ \mu s$, $f = 250$ Hz, $f_s = 5$ kHz, $I_m = 450$ A, and $I_a = 150$ A.

Solution

a. The rms value is defined as

$$I_r = \left[\frac{1}{T}\int_0^{t_1} (I_m \sin \omega_s t)^2\, dt + \frac{1}{T}\int_{t_2}^{t_3} I_a^2\, dt\right]^{1/2} = (I_{t1}^2 + I_{t2}^2)^{1/2} \tag{3.52}$$

where $\omega_s = 2\pi f_s = 31{,}415.93$ rad/s, $t_1 = \pi/\omega_s = 100\ \mu s$, and $T = 1/f$.

$$I_{r1} = \left[\frac{1}{T}\int_0^{t_1} (I_m \sin \omega_s t)^2\, dt\right]^{1/2} = I_m\sqrt{\frac{ft_1}{2}} = 50.31 \text{ A} \tag{3.53}$$

and

$$I_{r2} = \left(\frac{1}{T}\int_{t_2}^{t_3} I_a\, dt\right)^2 = I_a\sqrt{f(t_3 - t_2)} = 29.05 \text{ A} \tag{3.54}$$

Substituting Eqs. (3.53) and (3.54) in Eq. (3.52), the rms value is

$$I_r = \left[\frac{I_m^2 f t_1}{2} + I_a^2 f(t_3 - t_2)\right]^{1/2} = (50.31^2 + 29.05^2)^{1/2} = 58.09 \text{ A} \tag{3.55}$$

b. The average current is found from

$$I_d = \left[\frac{1}{T}\int_0^{t_1} (I_m \sin \omega_s t)\, dt + \frac{1}{T}\int_{t_2}^{t_3} I_a\, dt\right] = I_{d1} + I_{d2}$$

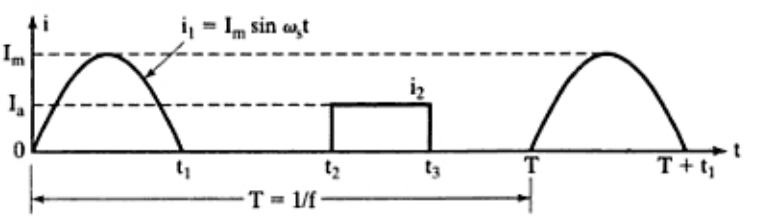


FIGURE 3.21
Current waveform.

where

$$I_{d1} = \frac{1}{T}\int_0^{t_1} (I_m \sin \omega_s t)\, dt = \frac{I_m f}{\pi f_s} \tag{3.56}$$

$$I_{d2} = \frac{1}{T}\int_{t_2}^{t_3} I_a\, dt = I_a f(t_3 - t_2) \tag{3.57}$$

Therefore, the average current becomes

$$I_{dc} = \frac{I_m f}{\pi f_s} + I_a f(t_3 - t_2) = 7.16 + 5.63 = 12.79 \text{ A}$$

Example 3.15 Finding the Load Inductance to Limit the Amount of Ripple Current

The single-phase bridge rectifier is supplied from a 120-V, 60-Hz source. The load resistance is $R = 500\ \Omega$. Calculate the value of a series inductor L that limits the rms ripple current I_{ac} to less than 5% of I_{dc}.

Solution

The load impedance

$$Z = R + j(n\omega L) = \sqrt{R^2 + (n\omega L)^2}\ \underline{/\theta_n} \tag{3.58}$$

and

$$\theta_n = \tan^{-1}\frac{n\omega L}{R} \tag{3.59}$$

and the instantaneous current is

$$i_0(t) = I_{dc} - \frac{4V_m}{\pi\sqrt{R^2 + (n\omega L)^2}}\left[\frac{1}{3}\cos(2\omega t - \theta_2) + \frac{1}{15}\cos(4\omega t - \theta_4)\ldots\right] \tag{3.60}$$

where

$$I_{dc} = \frac{V_{dc}}{R} = \frac{2V_m}{\pi R}$$

Equation (3.60) gives the rms value of the ripple current as

$$I_{ac}^2 = \frac{(4V_m)^2}{2\pi^2[R^2 + (2\omega L)^2]}\left(\frac{1}{3}\right)^2 + \frac{(4V_m)^2}{2\pi^2[R^2 + (4\omega L)^2]}\left(\frac{1}{15}\right)^2 + \cdots$$

Considering only the lowest order harmonic ($n = 2$), we have

$$I_{ac} = \frac{4V_m}{\sqrt{2}\pi\sqrt{R^2 + (2\omega L)^2}}\left(\frac{1}{3}\right)$$

Using the value of I_{dc} and after simplification, the ripple factor is

$$\text{RF} = \frac{I_{ac}}{I_{dc}} = \frac{0.4714}{\sqrt{1 + (2\omega L/R)^2}} = 0.05$$

For $R = 500\ \Omega$ and $f = 60$ Hz, the inductance value is obtained as $0.4714^2 = 0.05^2\,[1 + (4 \times 60 \times \pi L/500)^2]$ and this gives $L = 6.22$ H.

We can notice from Eq. (3.60) that an inductance in the load offers a high impedance for the harmonic currents and acts like a filter in reducing the harmonics. However, this inductance introduces a time delay of the load current with respect to the input voltage; and in the case of the single-phase half-wave rectifier, a freewheeling diode is required to provide a path for this inductive current.

Example 3.16 Finding the Filter Capacitance to Limit the Amount of Output Ripple Voltage

A single-phase bridge-rectifier is supplied from a 120-V, 60-Hz source. The load resistance is $R = 500\ \Omega$. (a) Design a C filter so that the ripple factor of the output voltage is less than 5%. (b) With the value of capacitor C in part (a), calculate the average load voltage V_{dc}.

Solution

a. When the instantaneous voltage v_s in Figure 3.22a is higher than the instantaneous capacitor voltage v_c, the diodes (D_1 and D_2 or D_3 and D_4) conduct; and the capacitor is then charged from the supply. If the instantaneous supply voltage v_s falls below the instantaneous capacitor voltage v_c, the diodes (D_1 and D_2 or D_3 and D_4) are reverse biased and the capacitor C_e discharges through the load resistance R. The capacitor voltage v_c varies between a minimum $V_{c(\min)}$ and maximum value $V_{c(\max)}$. This is shown in Figure 3.22b.

Let us assume that t_1 is the charging time and that t_2 is the discharging time of capacitor C_e. The equivalent circuit during charging is shown in Figure 3.22c. The capacitor charges almost instantaneously to the supply voltage v_s. The capacitor C_e will be charged to the peak supply voltage V_m, so that $v_c(t = t_1) = V_m$. Figure 3.22d shows the equivalent circuit during discharging. The capacitor discharges exponentially through R.

$$\frac{1}{C_e}\int i_0\,dt + v_c(t = 0) + Ri_0 = 0$$

which, with an initial condition of $v_c(t = 0) = V_m$, gives the discharging current as

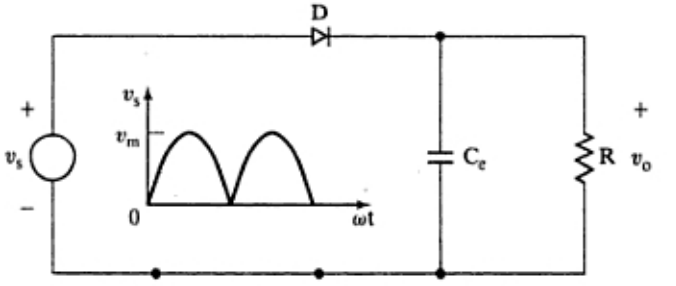
$$i_0 = \frac{V_m}{R}\,e^{-t/RC_e}$$

The output (or capacitor) voltage v_0 during the discharging period can be found from

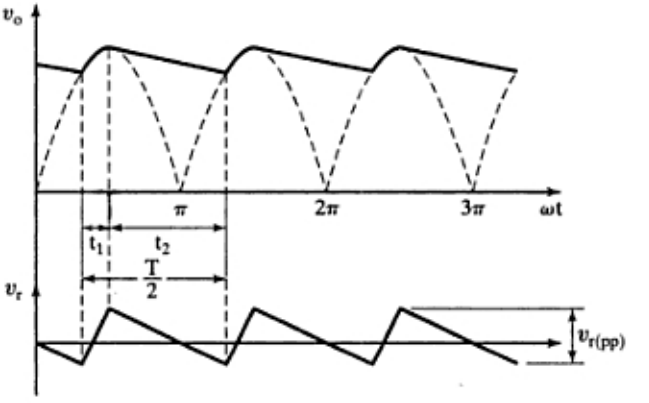
$$v_0(t) = Ri_0 = V_m e^{-t/RC_e}$$

The peak-to-peak ripple voltage $V_{r(\text{pp})}$ can be found from

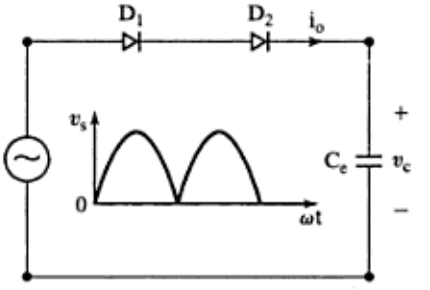
$$V_{r(\text{pp})} = v_0(t = t_1) - v_0(t = t_2) = V_m - V_m e^{-t_2/RC_e} = V_m(1 - e^{-t_2/RC_e}) \qquad (3.61)$$



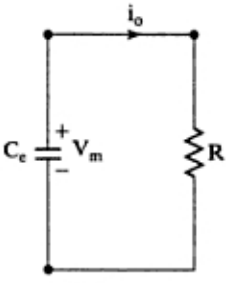
(a) Circuit model



(b) Waveforms for full-wave rectifier



(c) Charging



(d) Discharging

FIGURE 3.22

Single-phase bridge rectifier with *C* filter.

Since, $e^{-x} \approx 1 - x$, Eq. (3.61) can be simplified to

$$V_{r(pp)} = V_m\left(1 - 1 + \frac{t_2}{RC_e}\right) = \frac{V_m t_2}{RC_e} = \frac{V_m}{2fRC_e}$$

Therefore, the average load voltage V_{dc} is given by (assuming $t_2 = 1/2f$)

$$V_{dc} = V_m - \frac{V_{r(pp)}}{2} = V_m - \frac{V_m}{4fRC_e} \tag{3.62}$$

Thus, the rms output ripple voltage V_{ac} can be found approximately from

$$V_{ac} = \frac{V_{r(pp)}}{2\sqrt{2}} = \frac{V_m}{4\sqrt{2}fRC_e}$$

The RF can be found from

$$RF = \frac{V_{ac}}{V_{dc}} = \frac{V_m}{4\sqrt{2}fRC_e}\frac{4fRC_e}{V_m(4fRC_e - 1)} = \frac{1}{\sqrt{2}(4fRC_e - 1)} \tag{3.63}$$

which can be solved for C_e:

$$C_e = \frac{1}{4fR}\left(1 + \frac{1}{\sqrt{2}\,RF}\right) = \frac{1}{4 \times 60 \times 500}\left(1 + \frac{1}{\sqrt{2} \times 0.05}\right) = 126.2\ \mu F$$

b. From Eq. (3.62), the average load voltage V_{dc} is

$$V_{dc} = 169.7 - \frac{169.7}{4 \times 60 \times 500 \times 126.2 \times 10^{-6}} = 169.7 - 11.21 = 158.49\ V$$

Example 3.17 Finding the Values of an *LC* Output Filter to Limit the Amount of Output Ripple Voltage

An *LC* filter as shown in Figure 3.18c is used to reduce the ripple content of the output voltage for a single-phase full-wave rectifier. The load resistance is $R = 40\ \Omega$, load inductance is $L = 10$ mH, and source frequency is 60 Hz (or 377 rad/s). (a) Determine the values of L_e and C_e so that the RF of the output voltage is 10%. (b) Use PSpice to calculate Fourier components of the output voltage v_0. Assume diode parameters IS = 2-22E − 15, BV = 1800 V.

Solution

a. The equivalent circuit for the harmonics is shown in Figure 3.23. To make it easier for the nth harmonic ripple current to pass through the filter capacitor, the load impedance must be much greater than that of the capacitor. That is,

$$\sqrt{R^2 + (n\omega L)^2} \gg \frac{1}{n\omega C_e}$$

This condition is generally satisfied by the relation

$$\sqrt{R^2 + (n\omega L)^2} \simeq \frac{10}{n\omega C_e} \tag{3.64}$$

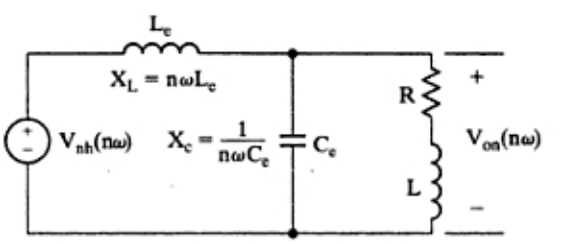


FIGURE 3.23
Equivalent circuit for harmonics.

and under this condition, the effect of the load is negligible. The rms value of the nth harmonic component appearing on the output can be found by using the voltage-divider rule and is expressed as

$$V_{on} = \left|\frac{-1/(n\omega C_e)}{(n\omega L_e) - 1/(n\omega C_e)}\right| V_{nh} = \left|\frac{-1}{(n\omega)^2 L_e C_e - 1}\right| V_{nh} \tag{3.65}$$

The total amount of ripple voltage due to all harmonics is

$$V_{ac} = \left(\sum_{n=2,4,6,\ldots}^{\infty} V_{on}^2\right)^{1/2} \tag{3.66}$$

For a specified value of V_{ac} and with the value of C_e from Eq. (3.64), the value of L_e can be computed. We can simplify the computation by considering only the dominant harmonic. From Eq. (3.22) we find that the second harmonic is the dominant one and its rms value is $V_{2h} = 4V_m/(3\sqrt{2}\pi)$ and the dc value, $V_{dc} = 2V_m/\pi$.

For $n = 2$, Eqs. (3.65) and (3.66) give

$$V_{ac} = V_{o2} = \left|\frac{-1}{(2\omega)^2 L_e C_e - 1}\right| V_{2h}$$

The value of the filter capacitor C_e is calculated from

$$\sqrt{R^2 + (2\omega L)^2} = \frac{10}{2\omega C_e}$$

or

$$C_e = \frac{10}{4\pi f\sqrt{R^2 + (4\pi f L)^2}} = 326\ \mu\text{F}$$

From Eq. (3.6) the RF is defined as

$$\text{RF} = \frac{V_{ac}}{V_{dc}} = \frac{V_{o2}}{V_{dc}} = \frac{V_{2h}}{V_{dc}}\frac{1}{(4\pi f)^2 L_e C_e - 1} = \frac{\sqrt{2}}{3}\left|\frac{1}{[(4\pi f)^2 L_e C_e - 1]}\right| = 0.1$$

or $(4\pi f)^2 L_e C_e - 1 = 4.714$ and $L_e = 30.83$ mH.

b. The single-phase bridge rectifier for PSpice simulation is shown in Figure 3.24. The list of the circuit file is as follows:

```
Example 3.17.  Single-Phase Bridge Rectifier with LC Filter
VS      1       0       SIN (0 169.7V 60HZ)
LE      3       8       30.83MH
CE      7       4       326UF
RX      8       7       80M                     ; Used to converge the solution
L       5       6       10MH
R       7       5       40
VX      6       4       DC 0V ; Voltage source to measure the output current
VY      1       2       DC 0V ; Voltage source to measure the input current
D1      2       3       DMOD                    ; Diode models
```

```
D2      4       0       DMOD
D3      0       3       DMOD
D4      4       2       DMOD
.MODEL  DMOD    D  (IS=2.22E-15 BV=1800V)  ; Diode model parameters
.TRAN   10US    50MS 33MS 50US             ; Transient analysis
.FOUR   120HZ   V(6,5)                     ; Fourier analysis of output voltage
.options  ITL5=0   abstol = 1.000u reltol = .05 vntol = 0.01m
.END
```

The results of PSpice simulation for the output voltage V(6,5) are as follows:

```
FOURIER COMPONENTS OF TRANSIENT RESPONSE V(6,5)
DC COMPONENT = 1.140973E+02
```

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.200E+02	1.304E+01	1.000E+00	1.038E+02	0.000E+00
2	2.400E+02	6.496E-01	4.981E-02	1.236E+02	1.988E+01
3	3.600E+02	2.277E-01	1.746E-02	9.226E+01	-1.150E+01
4	4.800E+02	1.566E-01	1.201E-02	4.875E+01	-5.501E+01
5	6.000E+02	1.274E-01	9.767E-03	2.232E+01	-8.144E+01
6	7.200E+02	1.020E-01	7.822E-03	8.358E+00	-9.540E+01
7	8.400E+02	8.272E-02	6.343E-03	1.997E+00	-1.018E+02
8	9.600E+02	6.982E-02	5.354E-03	-1.061E+00	-1.048E+02
9	1.080E+03	6.015E-02	4.612E-03	-3.436E+00	-1.072E+02

```
TOTAL HARMONIC DISTORTION = 5.636070E+00 PERCENT
```

which verifies the design.

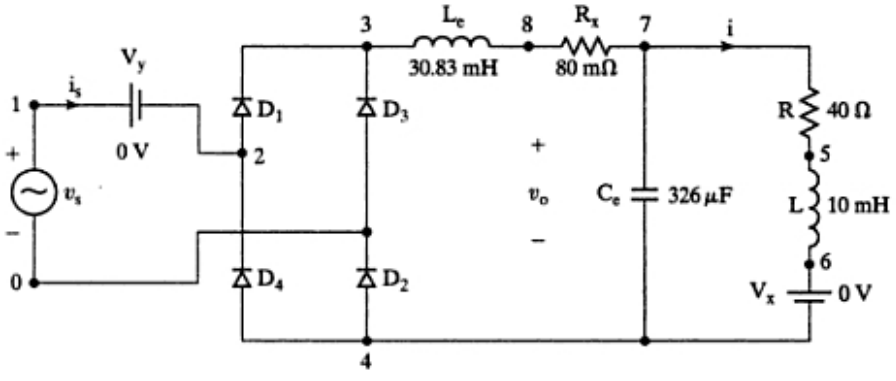


FIGURE 3.24

Single-phase bridge rectifier for PSpice simulation.

Example 3.18 Finding the Values of an *LC* Input Filter to Limit the Amount of Input Ripple Current

An *LC* input filter as shown in Figure 3.19 is used to reduce the input current harmonics in a single-phase full-wave rectifier of Figure 3.7a. The load current is ripple free and its average value is I_a. If the supply frequency is $f = 60$ Hz (or 377 rad/s), determine the resonant frequency of the filter so that the total input harmonic current is reduced to 1% of the fundamental component.

Solution

The equivalent circuit for the nth harmonic component is shown in Figure 3.25. The rms value of the nth harmonic current appearing in the supply is obtained by using the current-divider rule,

$$I_{sn} = \left|\frac{1/(n\omega C_i)}{(n\omega L_i - 1/(n\omega C_i)}\right| I_{nh} = \left|\frac{1}{(n\omega)^2 L_i C_i - 1}\right| I_{nh} \tag{3.67}$$

where I_{nh} is the rms value of the nth harmonic current. The total amount of harmonic current in the supply line is

$$I_h = \left(\sum_{n=2,3,\ldots}^{\infty} I_{sn}^2\right)^{1/2}$$

and the harmonic factor of input current (with the filter) is

$$r = \frac{I_h}{I_{s1}} = \left[\sum_{n=2,3,\ldots}^{\infty} \left(\frac{I_{sn}}{I_{s1}}\right)^2\right]^{1/2} \tag{3.68}$$

From Eq. (3.23), $I_{1h} = 4I_a/\sqrt{2}\,\pi$ and $I_{nh} = 4I_a/(\sqrt{2}\,n\pi)$ for $n = 3, 5, 7, \ldots$. From Eqs. (3.67) and (3.68) we get

$$r^2 = \sum_{n=3,5,7,\ldots}^{\infty} \left(\frac{I_{sn}}{I_{s1}}\right)^2 = \sum_{n=3,5,7,\ldots}^{\infty} \left|\frac{(w^2 L_i C_i - 1)^2}{n^2[(n\omega)^2 L_i C_i - 1]^2}\right| \tag{3.69}$$

This can be solved for the value of L_iC_i. To simplify the calculations, if we consider only the third harmonic, $3[(3 \times 2 \times \pi \times 60)^2 L_i C_i - 1]/(w^2 L_i C_i - 1) = 1/0.01 = 100$ or $L_iC_i = 9.349 \times 10^{-6}$ and the filter frequency is $1/\sqrt{L_iC_i} = 327.04$ rad/s, or 52.05 Hz. Assuming that $C_i = 1000\ \mu$F, we obtain $L_i = 9.349$ mH.

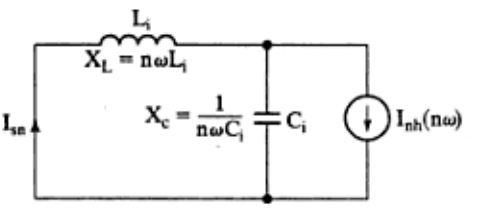


FIGURE 3.25
Equivalent circuit for harmonic current.

Note: The ac filter is generally tuned to the harmonic frequency involved, but it requires a careful design to avoid the possibility of resonance with the power system. The resonant frequency of the third-harmonic current is $377 \times 3 = 1131$ rad/s.

Key Points of Section 3.10

- The design of a rectifier requires determining the diode ratings and the ratings of filter components at the input and output side. Filters are used to smooth out the output voltage by a dc filter and to reduce the amount of harmonic injection to the input supply by an ac filter.

3.11 OUTPUT VOLTAGE WITH *LC* FILTER

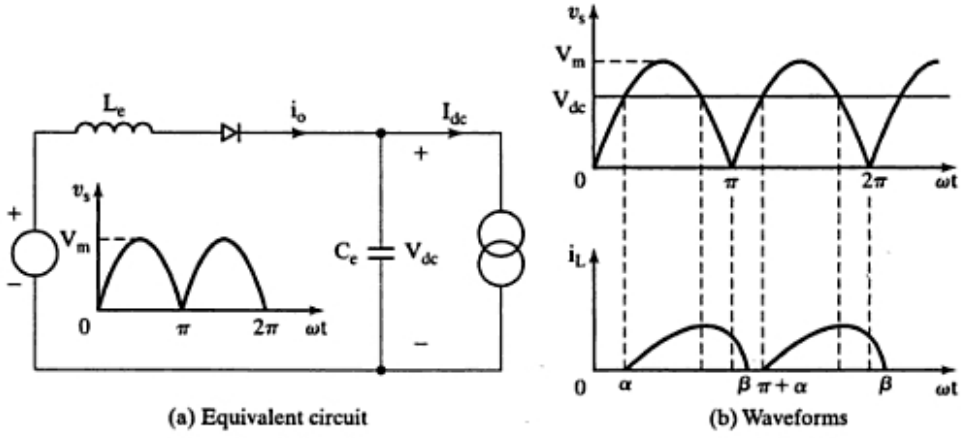
The equivalent circuit of a full-wave rectifier with an *LC* filter is shown in Figure 3.26a. Assume that the value of C_e is very large, so that its voltage is ripple free with an average value of $V_{o(dc)}$. L_e is the total inductance, including the source or line inductance, and is generally placed at the input side to act as an ac inductance instead of a dc choke.

If V_{dc} is less than V_m, the current i_0 begins to flow at α, which is given by

$$V_{dc} = V_m \sin \alpha$$

This in turn gives

$$\alpha = \sin^{-1} \frac{V_{dc}}{V_m} = \sin^{-1} x$$



(a) Equivalent circuit (b) Waveforms

FIGURE 3.26
Output voltage with *LC* filter.

where $x = V_{dc}/V_m$. The output current i_0 is given by

$$L_e \frac{di_L}{dt} = V_m \sin \omega t - V_{dc}$$

which can be solved for i_0.

$$\begin{aligned} i_0 &= \frac{1}{\omega L_e} \int_{\alpha}^{\omega_t} (V_m \sin \omega t - V_{dc})\, d(\omega t) \\ &= \frac{V_m}{\omega L_e}(\cos \alpha - \cos \omega t) - \frac{V_{dc}}{\omega L_e}(\omega t - \alpha) \qquad \text{for } \omega t \geq \alpha \end{aligned} \tag{3.70}$$

The critical value of $\omega t = \beta = \pi + \alpha$ at which the current i_0 falls to zero can be found from the condition $i_0(\omega t = \beta) = \pi + \alpha = 0$.

The average current I_{dc} can be found from

$$I_{dc} = \frac{1}{\pi} \int_{\alpha}^{\pi+\alpha} i_0(t)\, d(\omega t)$$

which, after integration and simplification gives

$$I_{dc} = \frac{V_m}{\omega L_e}\left[\sqrt{1 - x^2} + x\left(\frac{2}{\pi} - \frac{\pi}{2}\right)\right] \tag{3.71}$$

For $V_{dc} = 0$, the peak current that can flow through the rectifier is $I_{pk} = V_m/\omega L_e$. Normalizing I_{dc} with respect to I_{pk}, we get

$$k(x) = \frac{I_{dc}}{I_{pk}} = \sqrt{1 - x^2} + x\left(\frac{2}{\pi} - \frac{\pi}{2}\right) \tag{3.72}$$

Normalizing the rms value I_{rms} with respect to I_{pk}, we get

$$k_r(x) = \frac{I_{rms}}{I_{pk}} = \sqrt{\frac{1}{\pi} \int_{\alpha}^{\pi+\alpha} i_0(t)^2\, d(\omega \cdot t)} \tag{3.73}$$

Because α depends on the voltage ratio x, Eqs. (3.71) and (3.72) are dependent on x. Table 3.3 shows the values of $k(x)$ and $k_r(x)$ against the voltage ratio x.

Because the average voltage of the rectifier is $V_{dc} = 2\,V_m/\pi$, the average current equal to

$$I_{dc} = \frac{2\,V_m}{\pi R}$$

Thus,

$$\frac{2\,V_m}{\pi R} = I_{dc} = I_{pk}\, k(x) = \frac{V_m}{\omega L_e}\left[\sqrt{1 - x^2} + x\left(\frac{2}{\pi} - \frac{\pi}{2}\right)\right]$$

which gives the critical value of the inductance $L_{cr}(= L_e)$ for a continuous current as

$$L_{cr} = \frac{\pi R}{2\omega}\left[\sqrt{1 - x^2} + x\left(\frac{2}{\pi} - \frac{\pi}{2}\right)\right] \tag{3.74}$$

Thus, for a continuous current through the inductor, the value of L_e must be larger than the value of L_{cr}. That is,

$$L_e > L_{cr} = \frac{\pi R}{2\omega}\left[\sqrt{1 - x^2} + x\left(\frac{2}{\pi} - \frac{\pi}{2}\right)\right] \tag{3.75}$$

Discontinuous case. The current is discontinuous if $\omega t = \beta \leq (\pi + \alpha)$. The angle β at which the current is zero can be found by setting in Eq. (3.70) to zero. That is,

$$\cos(\alpha) - \cos(\beta) - x(\beta - \alpha) = 0$$

which in terms of x becomes

$$\sqrt{1 - x^2} - x(\beta - \arcsin(x)) = 0 \tag{3.76}$$

Example 3.19 Finding the Critical Value of Inductor for Continuous Load Current

The rms input voltage to the circuit in Figure 3.26a is 220 V, 60 Hz. (a) If the dc output voltage is $V_{dc} = 100$ V at $I_{dc} = 10$ A, determine the values of critical inductance L_e, α, and I_{rms}. (b) If $I_{dc} = 15$ A and $L_e = 6.5$ mH, use Table 3.3 to determine the values of V_{dc}, α, β, and I_{rms}.

TABLE 3.3 Normalized Load Current

x %	I_{dc}/I_{pk} %	I_{rms}/I_{pk} %	α Degrees	β Degrees
0	100.0	122.47	0	180
5	95.2	115.92	2.87	182.97
10	90.16	109.1	5.74	185.74
15	84.86	102.01	8.63	188.63
20	79.30	94.66	11.54	191.54
25	73.47	87.04	14.48	194.48
30	67.37	79.18	17.46	197.46
35	60.98	71.1	20.49	200.49
40	54.28	62.82	23.58	203.58
45	47.26	54.43	26.74	206.74
50	39.89	46.06	30.00	210.00
55	32.14	38.03	33.37	213.37
60	23.95	31.05	36.87	216.87
65	15.27	26.58	40.54	220.54
70	6.02	26.75	44.27	224.43
72	2.14	28.38	46.05	226.05
72.5	1.15	28.92	46.47	226.47
73	0.15	29.51	46.89	226.89
73.07	0	29.60	46.95	226.95

Solution

$\omega = 2\pi \times 60 = 377$ rad/s, $V_s = 120\,V$, $V_m = \sqrt{2} \times 120 = 169.7$ V.

a. Voltage ratio $x = V_{dc}/V_m = 100/169.7 = 58.93\%$; $\alpha = \sin^{-1}(x) = 36.87\%$. Equation (3.72) gives the average current ratio $k = I_{dc}/I_{pk} = 25.75\%$. Thus, $I_{pk} = I_{dc}/k = 10/0.2575 = 38.84$ A. The critical value of inductance is

$$L_{cr} = \frac{V_m}{\omega I_{pk}} = \frac{169.7}{377 \times 38.84} = 11.59 \text{ mH}$$

Equation (3.73) gives the rms current ratio $k_r = I_{rms}/I_{pk} = 32.4\%$. Thus,

$$I_{rms} = k_r I_{pk} = 0.324 \times 38.84 = 12.58 \text{ A}.$$

b. $L_e = 6.5$ mH, $I_{pk} = V_m/(\omega L_e) = 169.7/(377 \times 6.5 \text{ mH}) = 69.25$ A.

$$k = \frac{I_{dc}}{I_{pk}} = \frac{15}{69.25} = 21.66\%$$

Using linear interpolation, we get

$$x = x_n + \frac{(x_{n+1} - x_n)(k - k_n)}{k_{n+1} - k_n}$$

$$= 60 + \frac{(65 - 60)(21.66 - 23.95)}{15.27 - 23.95} = 61.32\%$$

$$V_{dc} = xV_m = 0.6132 \times 169.7 = 104.06 \text{ V}$$

$$\alpha = \alpha_n + \frac{(\alpha_{n+1} - \alpha_n)(k - k_n)}{k_{n+1} - k_n}$$

$$= 36.87 + \frac{(40.54 - 36.87)(21.66 - 23.95)}{15.27 - 23.95} = 37.84°$$

$$\beta = \beta_n + \frac{(\beta_{n+1} - \beta_n)(k - k_n)}{k_{n+1} - k_n}$$

$$= 216.87 + \frac{(220.54 - 216.87)(21.66 - 23.95)}{15.27 - 23.95} = 217.85°$$

$$k_r = \frac{I_{rms}}{I_{pk}} = k_{r(n)} + \frac{(k_{r(n+1)} - k_{r(n)})(k - k_n)}{k_{n+1} - k_n}$$

$$= 31.05 + \frac{(26.58 - 31.05)(21.66 - 23.95)}{15.27 - 23.95} = 29.87\%$$

Thus, $I_{rms} = 0.2987 \times I_{pk} = 0.2987 \times 69.25 = 20.68$ A.

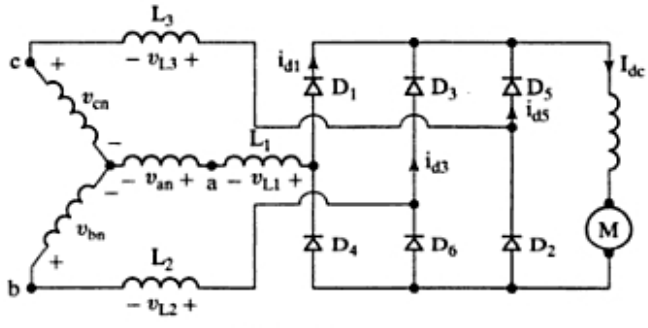
Key Points of Section 3.11

- With a high value of output filter capacitance C_e the output voltage remains almost constant. A minimum value of the filter inductance L_e is required to maintain a continuous current. The inductor L_e is generally placed at the input side to act as an ac inductor instead of a dc choke.

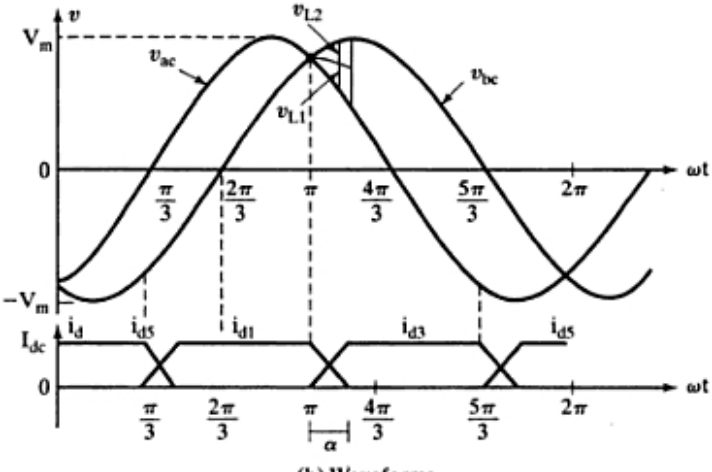
3.12 EFFECTS OF SOURCE AND LOAD INDUCTANCES

In the derivations of the output voltages and the performance criteria of rectifiers, it was assumed that the source has no inductances and resistances. However, in a practical transformer and supply, these are always present and the performances of rectifiers are slightly changed. The effect of the source inductance, which is more significant than that of resistance, can be explained with reference to Figure 3.27a.

The diode with the most positive voltage conducts. Let us consider the point $\omega t = \pi$ where voltages v_{ac} and v_{bc} are equal as shown in Figure 3.27b. The current I_{dc} is still flowing through diode D_1. Due to the inductance L_1, the current cannot fall to zero immediately and the transfer of current cannot be on an instantaneous basis. The current i_{d1} decreases, resulting in an induced voltage across L_1 of $+v_{01}$ and the output voltage becomes $v_0 = v_{ac} + v_{01}$. At the same time the current through D_3, i_{d3} increases from zero, inducing an equal voltage across L_2 of $-v_{02}$ and the output voltage becomes $v_{02} = v_{bc} - v_{02}$. The result is that the anode voltages of diodes D_1 and D_3 are equal;



(a) Circuit diagram



(b) Waveforms

FIGURE 3.27

Three-phase bridge rectifier with source inductances.

and both diodes conduct for a certain period which is called *commutation* (or *overlap*) *angle* μ. This transfer of current from one diode to another is called *commutation*. The reactance corresponding to the inductance is known as *commutating reactance*.

The effect of this overlap is to reduce the average output voltage of converters. The voltage across L_2 is

$$v_{L2} = L_2 \frac{di}{dt} \tag{3.77}$$

Assuming a linear rise of current i from 0 to I_{dc} (or a constant $di/dt = \Delta i/\Delta t$), we can write Eq. (3.77) as

$$v_{L2}\,\Delta t = L_2\,\Delta i \tag{3.78}$$

and this is repeated six times for a three-phase bridge rectifier. Using Eq. (3.78), the average voltage reduction due to the commutating inductances is

$$\begin{aligned} V_x &= \frac{1}{T} 2(v_{L1} + v_{L2} + v_{L3})\,\Delta t = 2f(L_1 + L_2 + L_3)\,\Delta i \\ &= 2f(L_1 + L_2 + L_3) I_{dc} \end{aligned} \tag{3.79}$$

If all the inductances are equal and $L_c = L_1 = L_2 = L_3$, Eq. (3.79) becomes

$$V_x = 6fL_cI_{dc} \tag{3.80}$$

where f is the supply frequency in hertz.

Example 3.20 Finding the Effect of Line Inductance on the Output Voltage of a Rectifier

A three-phase bridge rectifier is supplied from a Y-connected 208-V 60-Hz supply. The average load current is 60 A and has negligible ripple. Calculate the percentage reduction of output voltage due to commutation if the line inductance per phase is 0.5 mH.

Solution

$L_c = 0.5$ mH, $V_s = 208/\sqrt{3} = 120$ V, $f = 60$ Hz, $I_{dc} = 60$ A, and $V_m = \sqrt{2} \times 120 = 169.7$ V. From Eq. (3.40), $V_{dc} = 1.654 \times 169.7 = 280.7$ V. Equation (3.80) gives the output voltage reduction,

$$V_x = 6 \times 60 \times 0.5 \times 10^{-3} \times 60 = 10.8\text{ V} \quad \text{or} \quad 10.8 \times \frac{100}{280.7} = 3.85\%$$

and the effective output voltage is $(280.7 - 10.8) = 269.9$ V.

Example 3.21 Finding the Effect of Diode Recovery Time on the Output Voltage of a Rectifier

The diodes in the single-phase full-wave rectifier in Figure 3.6a have a reverse recovery time of $t_{rr} = 50$ μs and the rms input voltage is $V_s = 120$ V. Determine the effect of the reverse recovery time on the average output voltage if the supply frequency is (a) $f_s = 2$ kHz, and (b) $f_s = 60$ Hz.

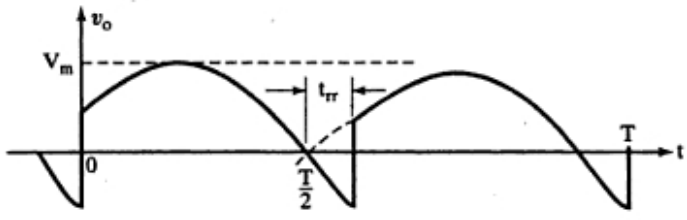


FIGURE 3.28
Effect of reverse recovery time on output voltage.

Solution

The reverse recovery time would affect the output voltage of the rectifier. In the full-wave rectifier of Figure 3.6a, the diode D_1 is not off at $\omega t = \pi$; instead, it continues to conduct until $t = \pi/\omega + t_{rr}$. As a result of the reverse recovery time, the average output voltage is reduced and the output voltage waveform is shown in Figure 3.28.

If the input voltage is $v = V_m \sin \omega t = \sqrt{2}\, V_s \sin \omega t$, the average output voltage reduction is

$$V_{rr} = \frac{2}{T}\int_0^{t_{rr}} V_m \sin \omega t\, dt = \frac{2V_m}{T}\left[-\frac{\cos \omega t}{\omega}\right]_0^{t_{rr}}$$
$$= \frac{V_m}{\pi}(1 - \cos \omega t_{rr})$$
$$V_m = \sqrt{2}\, V_s = \sqrt{2} \times 120 = 169.7 \text{ V} \qquad (3.81)$$

Without any reverse recovery time, Eq. (3.21) gives the average output voltage $V_{dc} = 0.6366V_m = 108.03$ V.

a. For $t_{rr} = 50\ \mu$s and $f_s = 2000$ Hz, the reduction of the average output voltage is

$$V_{rr} = \frac{V_m}{\pi}(1 - \cos 2\pi f_s t_{rr})$$
$$= 0.061V_m = 10.3 \text{ V} \quad \text{or} \quad 9.51\% \text{ of } V_{dc}$$

b. For $t_{rr} = 50\ \mu$s and $f_s = 60$ Hz, the reduction of the output dc voltage

$$V_{rr} = \frac{V_m}{\pi}(1 - \cos 2\pi f_s t_{rr}) = 5.65 \times 10^{-5} V_m$$
$$= 9.6 \times 10^{-3} \text{ V} \quad \text{or} \quad 8.88 \times 10^{-3}\% \text{ of } V_{dc}$$

Note: The effect of t_{rr} is significant for high-frequency source and for the case of normal 60-Hz source, its effect can be considered negligible.

Key Points of Section 3.12

- A practical supply has a source reactance. As a result, the transfer of current from one diode to another one cannot be instantaneous. There is an overlap known as

commutation angle, which lowers the effective output voltage of the rectifier. The effect of the diode reverse time may be significant for a high-frequency source.

SUMMARY

There are different types of rectifiers depending on the connections of diodes and input transformer. The performance parameters of rectifiers are defined and it has been shown that the performances of rectifiers vary with their types. The rectifiers generate harmonics into the load and the supply line; and these harmonics can be reduced by filters. The performances of the rectifiers are also influenced by the source and load inductances.

REFERENCES

[1] J. Schaefer, *Rectifier Circuits—Theory and Design*, New York: John Wiley & Sons, 1975.

[2] R. W. Lee, *Power Converter Handbook—Theory Design and Application*, Canadian General Electric, Peterborough, Ontario, 1979.

[3] Y.-S. Lee and M. H. L. Chow, *Power Electronics Handbook*, edited by M. H. Rashid. San Diego, CA: Academic Press, 2001, Chapter 10.

[4] IEEE Standard 597, *Practices and Requirements for General Purpose Thyristor Drives*, Piscataway, NJ, 1983.

REVIEW QUESTIONS

3.1 What is the turns ratio of a transformer?
3.2 What is a rectifier? What is the difference between a rectifier and a converter?
3.3 What is the blocking condition of a diode?
3.4 What are the performance parameters of a rectifier?
3.5 What is the significance of the form factor of a rectifier?
3.6 What is the significance of the ripple factor of a rectifier?
3.7 What is the efficiency of rectification?
3.8 What is the significance of the transformer utilization factor?
3.9 What is the displacement factor?
3.10 What is the input power factor?
3.11 What is the harmonic factor?
3.12 What is the difference between a half-wave and a full-wave rectifier?
3.13 What is the dc output voltage of a single-phase half-wave rectifier?
3.14 What is the dc output voltage of a single-phase full-wave rectifier?
3.15 What is the fundamental frequency of the output voltage of a single-phase full-wave rectifier?
3.16 What are the advantages of a three-phase rectifier over a single-phase rectifier?
3.17 What are the disadvantages of a multi-phase half-wave rectifier?
3.18 What are the advantages of a three-phase bridge rectifier over a six-phase star rectifier?
3.19 What are the purposes of filters in rectifier circuits?
3.20 What are the differences between ac and dc filters?
3.21 What are the effects of source inductances on the output voltage of a rectifier?
3.22 What are the effects of load inductances on the rectifier output?
3.23 What is a commutation of diodes?
3.24 What is the commutation angle of a rectifier?

PROBLEMS

3.1 A single-phase bridge rectifier has a purely resistive load $R = 10\ \Omega$, the peak supply voltage $V_m = 170$ V, and the supply frequency $f = 60$ Hz. Determine the average output voltage of the rectifier if the source inductance is negligible.

3.2 Repeat Problem 3.1 if the source inductance per phase (including transformer leakage inductance) is $L_c = 0.5$ mH.

3.3 A six-phase star rectifier has a purely resistive load of $R = 10\ \Omega$, the peak supply voltage $V_m = 170$ V, and the supply frequency $f = 60$ Hz. Determine the average output voltage of the rectifier if the source inductance is neglibile.

3.4 Repeat Problem 3.3 if the source inductance per phase (including the transformer leakage inductance) is $L_c = 0.5$ mH.

3.5 A three-phase bridge rectifier has a purely resistive load of $R = 100\ \Omega$ and is supplied from a 280-V, 60-Hz supply. The primary and secondary of the input transformer are connected in Y. Determine the average output voltage of the rectifier if the source inductances are negligible.

3.6 Repeat Problem 3.5 if the source inductance per phase (including transformer leakage inductance) is $L_c = 0.5$ mH.

3.7 The single-phase bridge rectifier of Figure 3.6a is required to supply an average voltage of $V_{dc} = 400$ V to a resistive load of $R = 10\ \Omega$. Determine the voltage and current ratings of diodes and transformer.

3.8 A three-phase bridge rectifier is required to supply an average voltage of $V_{dc} = 750$ V at a ripple-free current of $I_{dc} = 9000$ A. The primary and secondary of the transformer are connected in Y. Determine the voltage and current ratings of diodes and transformer.

3.9 The single-phase rectifier of Figure 3.5a has an RL load. If the peak input voltage is $V_m = 170$ V, the supply frequency $f = 60$ Hz, and the load resistance $R = 15\ \Omega$, determine the load inductance L to limit the load current harmonic to 4% of the average value I_{dc}.

3.10 The three-phase star rectifier of Figure 3.12a has an RL load. If the secondary peak voltage per phase is $V_m = 170$ V at 60 Hz, and the load resistance is $R = 15\ \Omega$, determine the load inductance L to limit the load current harmonics to 2% of the average value I_{dc}.

3.11 The battery voltage in Figure 3.4a is $E = 20$ V and its capacity is 200 Wh. The average charging current should be $I_{dc} = 10$ A. The primary input voltage is $V_p = 120$ V, 60 Hz, and the transformer has a turns ratio of $h = 2{:}1$. *Calculate* **(a)** the conduction angle δ of the diode, **(b)** the current-limiting resistance R, **(c)** the power rating P_R of R, **(d)** the charging time h in hours, **(e)** the rectifier efficiency η, and **(f)** the peak inverse voltage PIV of the diode.

3.12 The single-phase full-wave rectifier of Figure 3.8a has $L = 4.5$ mH, $R = 5\ \Omega$, and $E = 20$ V. The input voltage is $V_s = 120$ V at 60 Hz. **(a)** Determine (1) the steady-state load current I_0 at $\omega t = 0$, (2) the average diode current I_d, (3) the rms diode current I_r, and (4) the rms output current I_{rms}. **(b)** Use PSpice to plot the instantaneous output current i_0. Assume diode parameters IS = 2.22E − 15, BV = 1800 V.

3.13 The three-phase full-wave rectifier of Figure 3.13a has a load of $L = 2.5$ mH, $R = 5\ \Omega$, and $E = 20$ V. The line-to-line input voltage is $V_{ab} = 208$ V, 60 Hz. **(a)** Determine (1) the steady-state load current I_0 at $\omega t = \pi/3$, (2) the average diode current I_d, (3) the rms diode current I_r, and (4) the rms output current I_{rms}. **(b)** Use PSpice to plot the instantaneous output current i_0. Assume diode parameters IS = 2.22E − 15, BV = 1800 V.

3.14 A single-phase bridge rectifier is supplied from a 120-V, 60-Hz source. The load resistance is $R = 200\ \Omega$. **(a)** Design a C-filter so that the ripple factor of the output voltage is less than 5%. **(b)** With the value of capacitor C in part (a), calculate the average load voltage V_{dc}.

3.15 Repeat Problem 3.14 for the single-phase half-wave rectifier.

3.16 The rms input voltage to the circuit in Figure 3.22a is 120 V, 60 Hz. **(a)** If the dc output voltage is V_{dc} = 48 V at I_{dc} = 25 A, determine the values of inductance L_e, α, and I_{rms}. **(b)** If I_{dc} = 15 A and L_e = 6.5 mH, use Table 3.3 to calculate the values of V_{dc}, α, β, and I_{rms}.

3.17 The single-phase rectifier of Figure 3.15a has a resistive load of R, and a capacitor C is connected across the load. The average load current is I_{dc}. Assuming that the charging time of the capacitor is negligible compared with the discharging time, determine the rms output voltage harmonics, V_{ac}.

3.18 The LC filter shown in Figure 3.18c is used to reduce the ripple content of the output voltage for a six-phase star rectifier. The load resistance is R = 20 Ω, load inductance is L = 5 mH, and source frequency is 60 Hz. Determine the filter parameters L_e and C_e so that the ripple factor of the output voltage is 5%.

3.19 The three-phase bridge rectifier of Figure 3.3a has an RL load and is supplied from a Y connected supply. **(a)** Use the method of Fourier series to obtain expressions for the output voltage $v_0(t)$ and load current $i_0(t)$. **(b)** If peak phase voltage is V_m = 170 V at 60 Hz and the load resistance is R = 200 Ω, determine the load inductance L to limit the ripple current to 2% of the average value I_{dc}.

3.20 The single-phase half-wave rectifier of Figure 3.3a has a freewheeling diode and a ripple-free average load current of I_a. **(a)** Draw the waveforms for the currents in D_1, D_m, and the transformer primary; **(b)** express the primary current in Fourier series; and **(c)** determine the input PF and HF of the input current at the rectifier input. Assume a transformer turns ratio of unity.

3.21 The single-phase full-wave rectifier of Figure 3.5a has a ripple-free average load current of I_a. **(a)** Draw the waveforms for currents in D_1, D_2, and transformer primary; **(b)** express the primary current in Fourier series; and **(c)** determine the input PF and HF of the input current at the rectifier input. Assume a transformer turns ratio of unity.

3.22 The multiphase star rectifier of Figure 3.12a has three pulses and supplies a ripple-free average load current of I_a. The primary and secondary of the transformer are connected in Y. Assume a transformer turns ratio of unity. **(a)** Draw the waveforms for currents in D_1, D_2, D_3, and transformer primary; **(b)** express the primary current in Fourier series; and **(c)** determine the input PF and HF of input current.

3.23 Repeat Problem 3.22 if the primary of the transformer is connected in delta and secondary in Y.

3.24 The multiphase star rectifier of Figure 3.12a has six pulses and supplies a ripple-free average load current of I_a. The primary of the transformer is connected in delta and secondary in Y. Assume a transformer turns ratio of unity. **(a)** Draw the waveforms for currents in D_1, D_2, D_3, and transformer primary; **(b)** express the primary current in Fourier series; and **(c)** determine the input PF and HF of the input current.

3.25 The three-phase bridge rectifier of Figure 3.13a supplies a ripple-free load current of I_a. The primary and secondary of the transformer are connected in Y. Assume a transformer turns ratio of unity. **(a)** Draw the waveforms for currents in D_1, D_3, D_5 and the secondary phase current of the transformer; **(b)** express the secondary phase current in Fourier series; and **(c)** determine the input PF and HF of the input current.

3.26 Repeat Problem 3.25 if the primary of the transformer is connected in delta and secondary in Y.

3.27 Repeat Problem 3.25 if the primary and secondary of the transformer are connected in delta.

CHAPTER 4

Power Transistors

The learning objectives of this chapter are as follows:

- To learn the characteristics of an ideal switch
- To learn about different power transistors such as BJTs, MOSFETs, SITs, IGBTs, and COOLMOS.
- To learn the limitations of transistors as switches
- To understand the characteristics, gate control requirements, and models of power transistors

4.1 INTRODUCTION

Power transistors have controlled turn-on and turn-off characteristics. The transistors, which are used as switching elements, are operated in the saturation region, resulting in a low on-state voltage drop. The switching speed of modern transistors is much higher than that of thyristors and they are extensively employed in dc–dc and dc–ac converters, with inverse parallel-connected diodes to provide bidirectional current flow. However, their voltage and current ratings are lower than those of thyristors and transistors are normally used in low- to medium-power applications. The power transistors can be classified broadly into five categories:

1. Bipolar junction transistors (BJTs)
2. Metal oxide semiconductor field-effect transistors (MOSFETs)
3. Static induction transistors (SITs)
4. Insulated-gate bipolar transistors (IGBTs)
5. COOLMOS

BJTs, MOSFETs, SITs, IGBTs, or COOLMOS can be assumed as ideal switches to explain the power conversion techniques. A transistor can be operated as a switch. However, the choice between a BJT and an MOSFET in the converter circuits is not obvious, but each of them can replace a switch, provided that its voltage and current

ratings meet the output requirements of the converter. Practical transistors differ from ideal devices. The transistors have certain limitations and are restricted to some applications. The characteristics and ratings of each type should be examined to determine its suitability to a particular application.

4.2 BIPOLAR JUNCTION TRANSISTORS

A bipolar transistor is formed by adding a second *p*- or *n*-region to a *pn*-junction diode. With two *n*-regions and one *p*-region, two junctions are formed and it is known as an *NPN-transistor*, as shown in Figure 4.1a. With two *p*-regions and one *n*-region, it is called as a *PNP-transistor*, as shown in Figure 4.1b. The three terminals are named as *collector*, *emitter*, and *base*. A bipolar transistor has two junctions, collector–base junction (CBJ) and base–emitter junction (BEJ) [1–5] *NPN*-transistors of various sizes are shown in Figure 4.2.

There are two n^+-regions for the emitter of *NPN*-type transistor shown in Figure 4.3a and two p^+-regions for the emitter of the *PNP*-type transistor shown in Figure 4.3b. For an *NPN*-type, the emitter side *n*-layer is made wide, the *p*-base is narrow, and the collector side *n*-layer is narrow and heavily doped. For a *PNP*-type,

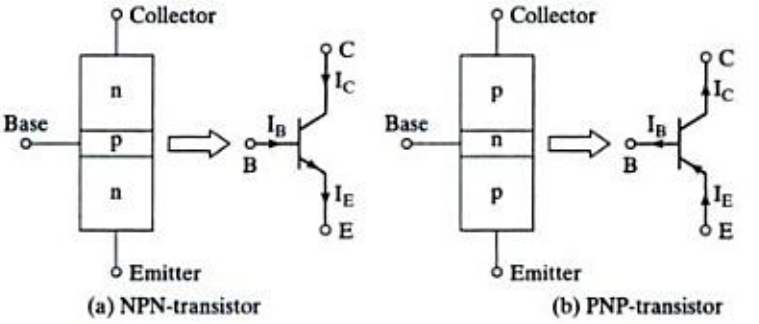


FIGURE 4.1
Bipolar transistors.

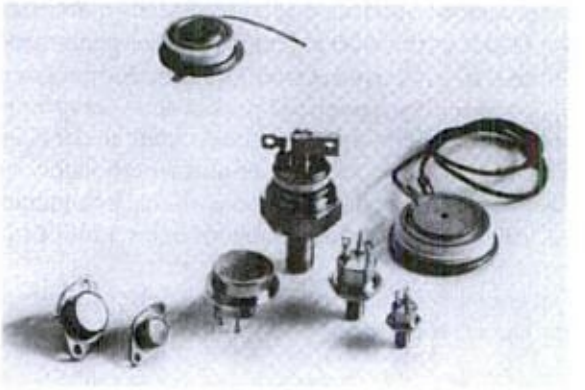


FIGURE 4.2
NPN-transistors. (Courtesy of Powerex, Inc.)

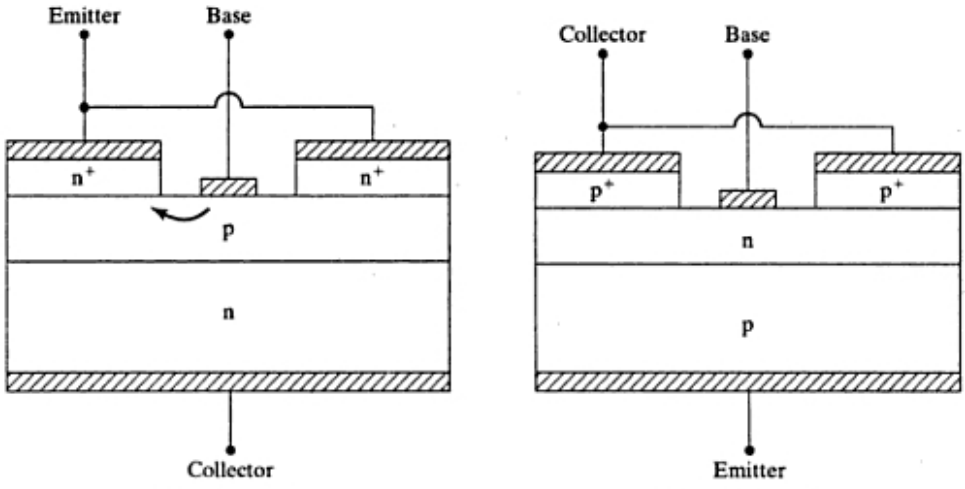


FIGURE 4.3
Cross sections of BJTs.

the emitter side p-layer is made wide, the n-base is narrow, and the collector side p-layer is narrow and heavily doped. The base and collector currents flow through two parallel paths, resulting in a low on-state collector–emitter resistance, $R_{CE(ON)}$.

4.2.1 Steady-State Characteristics

Although there are three possible configurations—common collector, common base, and common emitter, the common-emitter configuration, which is shown in Figure 4.4a for an *NPN*-transistor, is generally used in switching applications. The typical input characteristics of base current I_B, against base–emitter voltage V_{BE}, are shown in Figure 4.4b. Figure 4.4c shows the typical output characteristics of collector current I_C, against collector–emitter voltage V_{CE}. For a *PNP*-transistor, the polarities of all currents and voltages are reversed.

There are three operating regions of a transistor: cutoff, active, and saturation. In the cutoff region, the transistor is off or the base current is not enough to turn it on and both junctions are reverse biased. In the active region, the transistor acts as an amplifier, where the base current is amplified by a gain and the collector–emitter voltage decreases with the base current. The CBJ is reverse biased, and the BEJ is forward biased. In the saturation region, the base current is sufficiently high so that the collector–emitter voltage is low, and the transistor acts as a switch. Both junctions (CBJ and BEJ) are forward biased. The transfer characteristic, which is a plot of V_{CE} against I_B, is shown in Figure 4.5.

The model of an *NPN*-transistor is shown in Figure 4.6 under large-signal dc operation. The equation relating the currents is

$$I_E = I_C + I_B \tag{4.1}$$

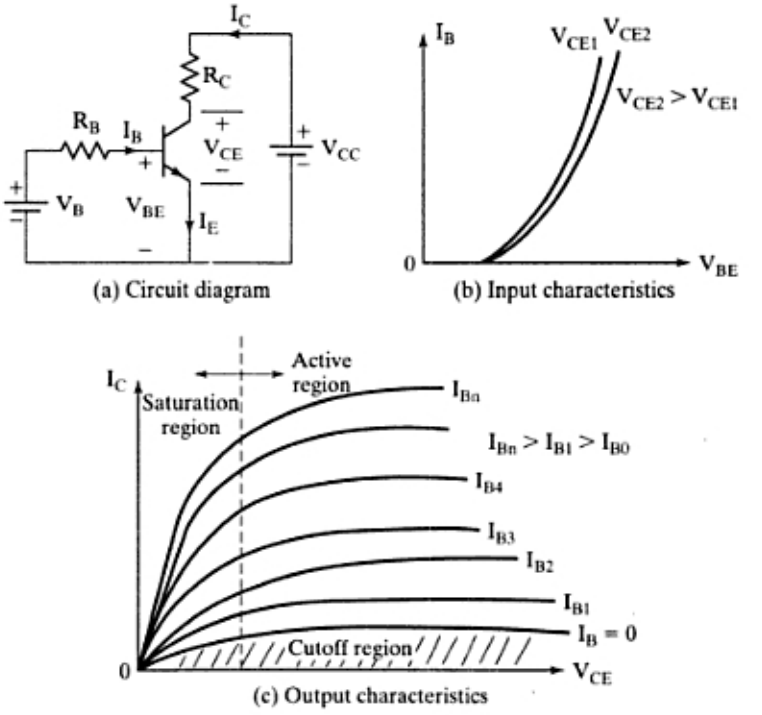


FIGURE 4.4

Characteristics of *NPN*-transistors.

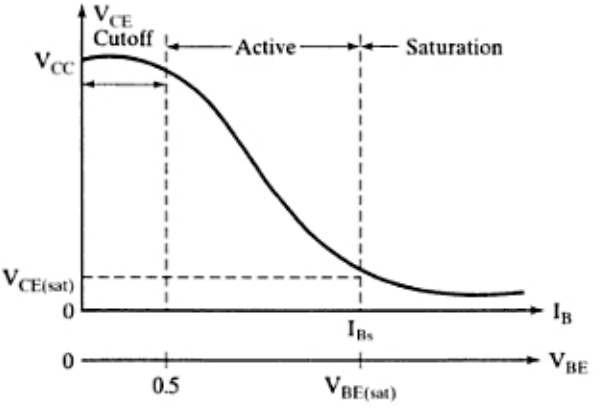


FIGURE 4.5

Transfer characteristics.

The base current is effectively the input current and the collector current is the output current. The ratio of the collector current I_C, to base current I_B, is known as the forward *current gain*, β_F:

$$\beta_F = h_{FE} = \frac{I_C}{I_B} \tag{4.2}$$

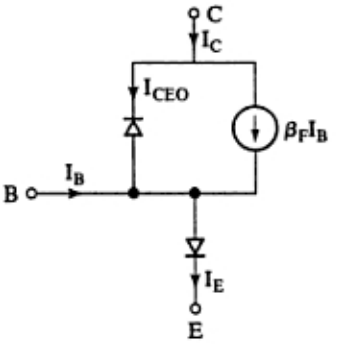


FIGURE 4.6
Model of *NPN*-transistors.

The collector current has two components: one due to the base current and the other is the leakage current of the CBJ.

$$I_C = \beta_F I_B + I_{CEO} \tag{4.3}$$

where I_{CEO} is the collector-to-emitter leakage current with base open circuit and can be considered negligible compared to $\beta_F I_B$.

From Eqs. (4.1) and (4.3),

$$I_E = I_B(1 + \beta_F) + I_{CEO} \tag{4.4}$$

$$\approx I_B(1 + \beta_F) \tag{4.4a}$$

$$I_E \approx I_C\left(1 + \frac{1}{\beta_F}\right) = I_C\frac{\beta_F + 1}{\beta_F} \tag{4.5}$$

Because $\beta_F \gg 1$, the collector current can be expressed as

$$I_C \approx \alpha_F I_E \tag{4.6}$$

where the constant α_F is related to β by

$$\alpha_F = \frac{\beta_F}{\beta_F + 1} \tag{4.7}$$

or

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F} \tag{4.8}$$

Let us consider the circuit of Figure 4.7, where the transistor is operated as a switch.

$$I_B = \frac{V_B - V_{BE}}{R_B} \tag{4.9}$$

$$V_C = V_{CE} = V_{CC} - I_C R_C = V_{CC} - \frac{\beta_F R_C}{R_B}(V_B - V_{BE})$$

$$V_{CE} = V_{CB} + V_{BE} \tag{4.10}$$

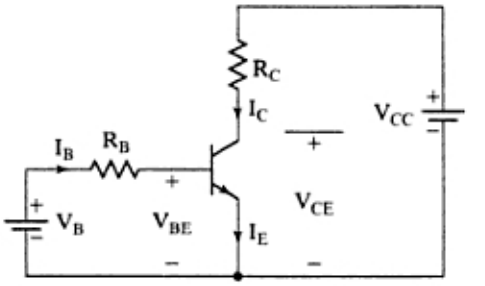


FIGURE 4.7
Transistor switch.

or

$$V_{CB} = V_{CE} - V_{BE} \tag{4.11}$$

Equation (4.11) indicates that as long as $V_{CE} \geq V_{BE}$, the CBJ is reverse biased and the transistor is in the active region. The maximum collector current in the active region, which can be obtained by setting $V_{CB} = 0$ and $V_{BE} = V_{CE}$, is

$$I_{CM} = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC} - V_{BE}}{R_C} \tag{4.12}$$

and the corresponding value of base current

$$I_{BM} = \frac{I_{CM}}{\beta_F} \tag{4.13}$$

If the base current is increased above I_{BM}, V_{BE} increases, the collector current increases, and the V_{CE} falls below V_{BE}. This continues until the CBJ is forward biased with V_{BC} of about 0.4 to 0.5 V. The transistor then goes into saturation. The *transistor saturation* may be defined as the point above which any increase in the base current does not increase the collector current significantly.

In the saturation, the collector current remains almost constant. If the collector–emitter saturation voltage is $V_{CE(sat)}$, the collector current is

$$I_{CS} = \frac{V_{CC} - V_{CE(sat)}}{R_C} \tag{4.14}$$

and the corresponding value of base current is

$$I_{BS} = \frac{I_{CS}}{\beta_F} \tag{4.15}$$

Normally, the circuit is designed so that I_B is higher than I_{BS}. The ratio of I_B to I_{BS} is called the *overdrive factor* (ODF):

$$\text{ODF} = \frac{I_B}{I_{BS}} \tag{4.16}$$

and the ratio of I_{CS} to I_B is called as *forced* β, β_{forced} where

$$\beta_{forced} = \frac{I_{CS}}{I_B} \tag{4.17}$$

The total power loss in the two junctions is

$$P_T = V_{BE}I_B + V_{CE}I_C \tag{4.18}$$

A high value of ODF cannot reduce the collector–emitter voltage significantly. However, V_{BE} increases due to increased base current, resulting in increased power loss in the BEJ.

Example 4.1 Finding the Saturation Parameters of a BJT

The bipolar transistor in Figure 4.7 is specified to have β_F in the range of 8 to 40. The load resistance is $R_C = 11\ \Omega$. The dc supply voltage is $V_{CC} = 200$ V and the input voltage to the base circuit is $V_B = 10$ V. If $V_{CE(sat)} = 1.0$ V and $V_{BE(sat)} = 1.5$ V, find (a) the value of R_B that results in saturation with an ODF of 5, (b) the β_{forced}, and (c) the power loss P_T in the transistor.

Solution

$V_{CC} = 200$ V, $\beta_{min} = 8$, $\beta_{max} = 40$, $R_C = 11\ \Omega$, ODF = 5, $V_B = 10$ V, $V_{CE(sat)} = 1.0$ V, and $V_{BE(sat)} = 1.5$ V. From Eq. (4.14), $I_{CS} = (200 - 1.0)/11 = 18.1$ A. From Eq. (4.15), $I_{BS} = 18.1/\beta_{min} = 18.1/8 = 2.2625$ A. Equation (4.16) gives the base current for an overdrive factor of 5,

$$I_B = 5 \times 2.2625 = 11.3125 \text{ A}$$

a. Equation (4.9) gives the required value of R_B,

$$R_B = \frac{V_B - V_{BE(sat)}}{I_B} = \frac{10 - 1.5}{11.3125} = 0.7514\ \Omega$$

b. From Eq. (4.17), $\beta_{forced} = 18.1/11.3125 = 1.6$.

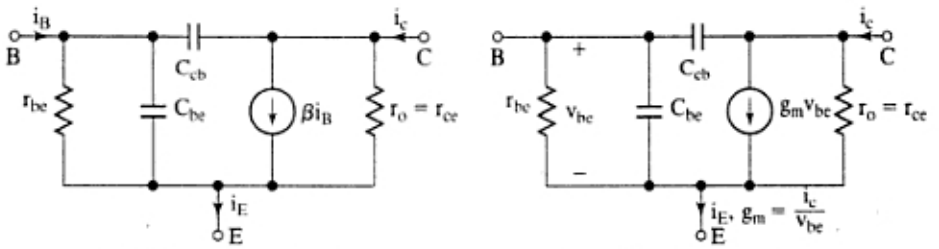
c. Equation (4.18) yields the total power loss as

$$P_T = 1.5 \times 11.3125 + 1.0 \times 18.1 = 16.97 + 18.1 = 35.07 \text{ W}$$

Note: For an ODF of 10, $I_B = 22.265$ A and the power loss is $P_T = 1.5 \times 22.265 + 18.1 = 51.5$ W. Once the transistor is saturated, the collector–emitter voltage is not reduced in relation to the increase in base current. However, the power loss is increased. At a high value of ODF, the transistor may be damaged due to thermal runaway. On the other hand, if the transistor is underdriven ($I_B < I_{CB}$), it may operate in the active region and V_{CE} increases, resulting in increased power loss.

4.2.2 Switching Characteristics

A forward-biased *pn*-junction exhibits two parallel capacitances: a depletion-layer capacitance and a diffusion capacitance. On the other hand, a reverse-biased *pn*-junction has only depletion capacitance. Under steady-state conditions, these capacitances do



(a) Model with current gain (b) Model with transconductance

FIGURE 4.8

Transient model of BJT.

not play any role. However, under transient conditions, they influence the turn-on and turn-off behavior of the transistor.

The model of a transistor under transient conditions is shown in Figure 4.8, where C_{cb} and C_{be} are the effective capacitances of the CBJ and BEJ, respectively. The *transconductance*, g_m, of a BJT is defined as the ratio of ΔI_C to ΔV_{BE}. These capacitances are dependent on junction voltages and physical construction of the transistor. C_{cb} affects the input capacitance significantly due to the Miller multiplication effect [6]. The resistances of collector to emitter and base to emitter, are r_{ce} and r_{be}, respectively.

Due to internal capacitances, the transistor does not turn on instantly. Figure 4.9 illustrates the waveforms and switching times. As the input voltage v_B rises from zero to V_1 and the base current rises to I_{B1}, the collector current does not respond immediately. There is a delay, known as *delay time*, t_d before any collector current flows. This delay is required to charge up the capacitance of the BEJ to the forward-bias voltage V_{BE} (approximately 0.7 V). After this delay, the collector current rises to the steady-state value of I_{CS}. The rise time t_r depends on the time constant determined by BEJ capacitance.

The base current is normally more than that required to saturate the transistor. As a result, the excess minority carrier charge is stored in the base region. The higher the ODF, the greater is the amount of extra charge stored in the base. This extra charge, which is called the *saturating charge*, is proportional to the excess base drive and the corresponding current I_e:

$$I_e = I_B - \frac{I_{CS}}{\beta} = \text{ODF} \cdot I_{BS} - I_{BS} = I_{BS}(\text{ODF} - 1) \tag{4.19}$$

and the saturating charge is given by

$$Q_s = \tau_s I_e = \tau_s I_{BS}(\text{ODF} - 1) \tag{4.20}$$

where τ_s is known as the *storage time constant* of the transistor.

When the input voltage is reversed from V_1 to $-V_2$ and the base current is also changed to $-I_{B2}$, the collector current does not change for a time t_s, called the *storage time*. The t_s is required to remove the saturating charge from the base. Because v_{BE} is still positive with approximately 0.7 V only, the base current reverses its direction due

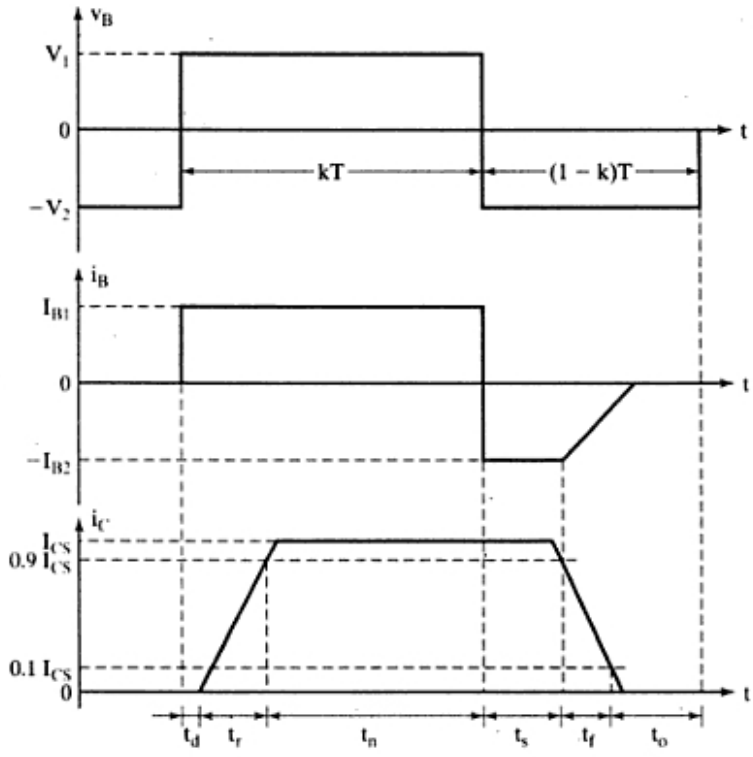


FIGURE 4.9

Switching times of bipolar transistors.

to the change in the polarity of v_B from V_1 to $-V_2$. The reverse current, $-I_{B2}$, helps to discharge the base and remove the extra charge from the base. Without $-I_{B2}$, the saturating charge has to be removed entirely by recombination and the storage time would be longer.

Once the extra charge is removed, the BEJ capacitance charges to the input voltage $-V_2$, and the base current falls to zero. The fall time t_f depends on the time constant, which is determined by the capacitance of the reverse-biased BEJ.

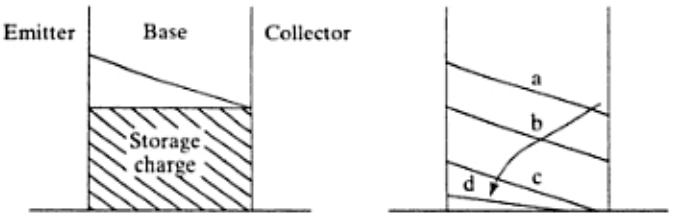
Figure 4.10a shows the extra storage charge in the base of a saturated transistor. During turn-off, this extra charge is removed first in time t_s and the charge profile is changed from a to c as shown in Figure 4.10b. During fall time, the charge profile decreases from profile c until all charges are removed.

The turn-on time t_{on} is the sum of delay time t_d and rise time t_r:

$$t_{on} = t_d + t_r$$

and the turn-off time t_{off} is the sum of storage time t_s and fall time t_f:

$$t_{off} = t_s + t_f$$



(a) Charge storage in base (b) Charge profile during turn-off

FIGURE 4.10

Charge storage in saturated bipolar transistors.

Example 4.2 Finding the Switching Loss of a BJT

The waveforms of the transistor switch in Figure 4.7 are shown in Figure 4.11. The parameters are $V_{CC} = 250$ V, $V_{BE(sat)} = 3$ V, $I_B = 8$ A, $V_{CS(sat)} = 2$ V, $I_{CS} = 100$ A, $t_d = 0.5$ μs, $t_r = 1$ μs, $t_s = 5$ μs, $t_f = 3$ μs, and $f_s = 10$ kHz. The duty cycle is $k = 50\%$. The collector-to-emitter leakage current is $I_{CEO} = 3$ mA. Determine the power loss due to collector current (a) during turn-on $t_{on} = t_d + t_r$, (b) during conduction period t_n, (c) during turn-off $t_{off} = t_s + t_f$, (d) during off-time t_o, and (e) total average power losses P_T. (f) Plot the instantaneous power due to collector current $P_c(t)$.

Solution

$T = 1/f_s = 100$ μs, $k = 0.5$, $kT = t_d + t_r + t_n = 50$ μs, $t_n = 50 - 0.5 - 1 = 48.5$ μs, $(1 - k)T = t_s + t_f + t_o = 50$ μs, and $t_o = 50 - 5 - 3 = 42$ μs.

a. During delay time, $0 \le t \le t_d$:

$$i_c(t) = I_{CEO}$$
$$v_{CE}(t) = V_{CC}$$

The instantaneous power due to the collector current is

$$P_c(t) = i_c v_{CE} = I_{CEO} V_{CC}$$
$$= 3 \times 10^{-3} \times 250 = 0.75 \text{ W}$$

The average power loss during the delay time is

$$P_d = \frac{1}{T}\int_0^{t_d} P_c(t)dt = I_{CEO} V_{CC} t_d f_s \tag{4.21}$$
$$= 3 \times 10^{-3} \times 250 \times 0.5 \times 10^{-6} \times 10 \times 10^3 = 3.75 \text{ mW}$$

During rise time, $0 \le t \le t_r$:

$$i_c(t) = \frac{I_{CS}}{t_r} t$$
$$v_{CE}(t) = V_{CC} + (V_{CE(sat)} - V_{CC})\frac{t}{t_r}$$

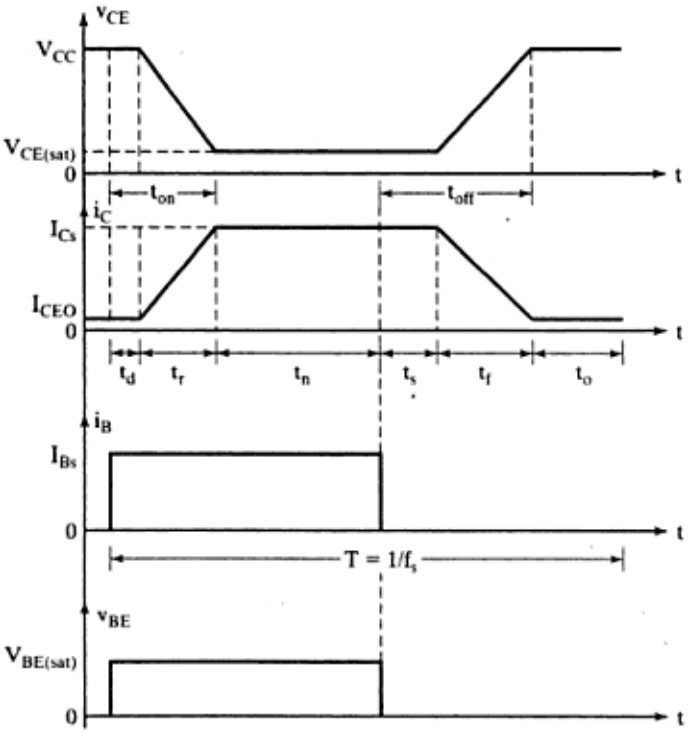


FIGURE 4.11
Waveforms of transistor switch.

$$P_c(t) = i_c v_{CE} = I_{CS}\frac{t}{t_r}\left[V_{CC} + (V_{CE\,(sat)} - V_{CC})\frac{t}{t_r}\right] \tag{4.22}$$

The power $P_c(t)$ is maximum when $t = t_m$, where

$$\begin{aligned} t_m &= \frac{t_r V_{CC}}{2[V_{CC} - V_{CE\,(sat)}]} \\ &= 1 \times \frac{250}{2(250 - 2)} = 0.504\ \mu s \end{aligned} \tag{4.23}$$

and Eq. (4.22) yields the peak power

$$\begin{aligned} P_p &= \frac{V_{CC}^2 I_{CS}}{4[V_{CC} - V_{CE(sat)}]} \\ &= 250^2 \times \frac{100}{4(250 - 2)} = 6300\ \text{W} \end{aligned} \tag{4.24}$$

$$P_r = \frac{1}{T}\int_0^{t_r} P_c(t)dt = f_s I_{CS} t_r \left[\frac{V_{CC}}{2} + \frac{V_{CE(sat)} - V_{CC}}{3}\right] \tag{4.25}$$
$$= 10 \times 10^3 \times 100 \times 1 \times 10^{-6}\left[\frac{250}{2} + \frac{2 - 250}{3}\right] = 42.33 \text{ W}$$

The total power loss during the turn-on is

$$P_{on} = P_d + P_r \tag{4.26}$$
$$= 0.00375 + 42.33 = 42.33 \text{ W}$$

b. The conduction period, $0 \le t \le t_n$:

$$i_c(t) = I_{CS}$$
$$v_{CE}(t) = V_{CE(sat)}$$
$$P_c(t) = i_c v_{CE} = V_{CE(sat)} I_{CS}$$
$$= 2 \times 100 = 200 \text{ W}$$
$$P_n = \frac{1}{T}\int_0^{t_n} P_c(t)dt = V_{CE(sat)} I_{CS} t_n f_s \tag{4.27}$$
$$= 2 \times 100 \times 48.5 \times 10^{-6} \times 10 \times 10^3 = 97 \text{ W}$$

c. The storage period, $0 \le t \le t_s$:

$$i_c(t) = I_{CS}$$
$$v_{CE}(t) = V_{CE(sat)}$$
$$P_c(t) = i_c v_{CE} = V_{CE(sat)} I_{CS}$$
$$= 2 \times 100 = 200 \text{ W}$$
$$P_s = \frac{1}{T}\int_0^{t_s} P_c(t)dt = V_{CE(sat)} I_{CS} t_s f_s \tag{4.28}$$
$$= 2 \times 100 \times 5 \times 10^{-6} \times 10 \times 10^3 = 10 \text{ W}$$

The fall time, $0 \le t \le t_f$:

$$i_c(t) = I_{CS}\left(1 - \frac{t}{t_f}\right), \text{ neglecting } I_{CEO}$$
$$v_{CE}(t) = \frac{V_{CC}}{t_f} t, \text{ neglecting } I_{CEO} \tag{4.29}$$
$$P_c(t) = i_c v_{CE} = V_{CC} I_{CS}\left[\left(1 - \frac{t}{t_f}\right)\frac{t}{t_f}\right]$$

This power loss during fall time is maximum when $t = t_f/2 = 1.5$ μs and Eq. (4.29) gives the peak power,

$$P_m = \frac{V_{CC} I_{CS}}{4} \tag{4.30}$$
$$= 250 \times \frac{100}{4} = 6250 \text{ W}$$

$$P_f = \frac{1}{T}\int_0^{t_f} P_c(t)dt = \frac{V_{CC}I_{CS}t_f f_s}{6}$$
$$= \frac{250 \times 100 \times 3 \times 10^{-6} \times 10 \times 10^3}{6} = 125 \text{ W} \tag{4.31}$$

The power loss during turn-off is

$$P_{\text{off}} = P_s + P_f = I_{CS}f_s\left(t_s V_{CE(\text{sat})} + \frac{V_{CC}t_f}{6}\right)$$
$$= 10 + 125 = 135 \text{ W} \tag{4.32}$$

d. Off-period, $0 \le t \le t_o$:

$$i_c(t) = I_{CEO}$$
$$v_{CE}(t) = V_{CC}$$
$$P_c(t) = i_c v_{CE} = I_{CEO}V_{CC} \tag{4.33}$$
$$= 3 \times 10^{-3} \times 250 = 0.75 \text{ W}$$
$$P_0 = \frac{1}{T}\int_0^{t_o} P_c(t)dt = I_{CEO}V_{CC}t_o f_s$$
$$= 3 \times 10^{-3} \times 250 \times 42 \times 10^{-6} \times 10 \times 10^3 = 0.315 \text{ W}$$

e. The total power loss in the transistor due to collector current is

$$P_T = P_{\text{on}} + P_n + P_{\text{off}} + P_0$$
$$= 42.33 + 97 + 135 + 0.315 = 274.65 \text{ W} \tag{4.34}$$

f. The plot of the instantaneous power is shown in Figure 4.12

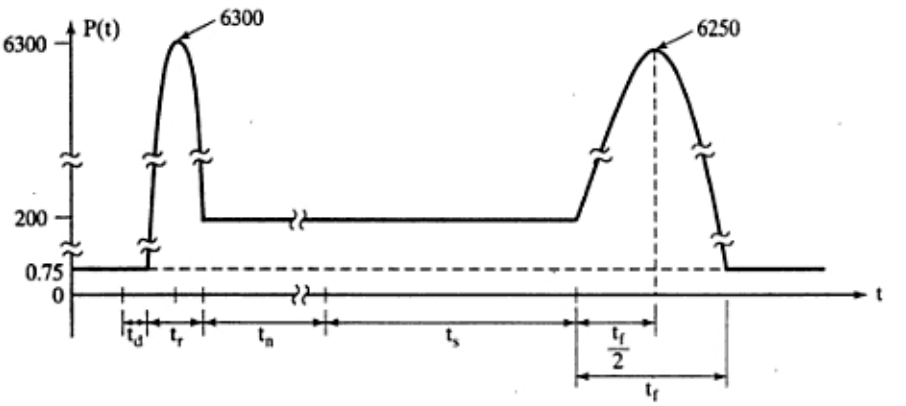


FIGURE 4.12

Plot of instantaneous power for Example 4.2.

Example 4.3 Finding the Base Drive Loss of a BJT

For the parameters in Example 4.2, calculate the average power loss due to the base current.

Solution

$V_{BE(sat)} = 3$ V, $I_B = 8$ A, $T = 1/f_s = 100$ μs, $k = 0.5$, $kT = 50$ μs, $t_d = 0.5$ μs, $t_r = 1$ μs, $t_n = 50 - 1.5 = 48.5$ μs, $t_s = 5$ μs, $t_f = 3$ μs, $t_{on} = t_d + t_r = 1.5$ μs, and $t_{off} = t_s + t_f = 5 + 3 = 8$ μs.

During the period, $0 \le t \le (t_{on} + t_n)$:

$$i_b(t) = I_{BS}$$
$$v_{BE}(t) = V_{BE(sat)}$$

The instantaneous power due to the base current is

$$P_b(t) = i_b v_{BE} = I_{BS} V_{BS(sat)}$$
$$= 8 \times 3 = 24 \text{ W}$$

During the period, $0 \le t \le t_o = (T - t_{on} - t_n - t_s - t_f)$: $P_b(t) = 0$. The average power loss is

$$P_B = I_{BS} V_{BE(sat)} (t_{on} + t_n + t_s + t_f) f_s$$
$$= 8 \times 3 \times (1.5 + 48.5 + 5 + 3) \times 10^{-6} \times 10 \times 10^3 = 13.92 \text{ W} \quad (4.35)$$

4.2.3 Switching Limits

Second breakdown (SB). The SB, which is a destructive phenomenon, results from the current flow to a small portion of the base, producing localized hot spots. If the energy in these hot spots is sufficient, the excessive localized heating may damage the transistor. Thus, secondary breakdown is caused by a localized thermal runaway, resulting from high current concentrations. The current concentration may be caused by defects in the transistor structure. The SB occurs at certain combinations of voltage, current, and time. Because the time is involved, the secondary breakdown is basically an energy dependent phenomenon.

Forward-biased safe operating area (FBSOA). During turn-on and on-state conditions, the average junction temperature and second breakdown limit the power-handling capability of a transistor. The manufacturers usually provide the FBSOA curves under specified test conditions. FBSOA indicates the i_c–v_{CE} limits of the transistor; and for reliable operation the transistor must not be subjected to greater power dissipation than that shown by the FBSOA curve.

Reverse-biased safe operating area (RBSOA). During turn-off, a high current and high voltage must be sustained by the transistor, in most cases with the base-to-emitter junction reverse biased. The collector–emitter voltage must be held to a safe level at, or below, a specified value of collector current. The manufacturers provide the I_C–V_{CE} limits during reverse-biased turn-off as RBSOA.

Power derating. The thermal equivalent circuit is shown in Figure 4.13. If the total average power loss is P_T, the case temperature is

$$T_C = T_J - P_T R_{JC}$$

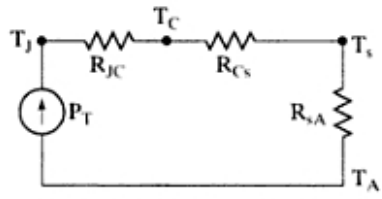


FIGURE 4.13
Thermal equivalent circuit of a transistor.

The sink temperature is

$$T_S = T_C - P_T R_{CS}$$

The ambient temperature is

$$T_A = T_S - P_T R_{SA}$$

and

$$T_J - T_A = P_T(R_{JC} + R_{CS} + R_{SA}) \tag{4.36}$$

where R_{JC} = thermal resistance from junction to case, °C/W;
R_{CS} = thermal resistance from case to sink, °C/W;
R_{SA} = thermal resistance from sink to ambient, °C/W.

The maximum power dissipation P_T is normally specified at $T_C = 25°C$. If the ambient temperature is increased to $T_A = T_{J(\max)} = 150°C$, the transistor can dissipate zero power. On the other hand, if the junction temperature is $T_C = 0°C$, the device can dissipate maximum power and this is not practical. Therefore, the ambient temperature and thermal resistances must be considered when interpreting the ratings of devices. Manufacturers show the derating curves for the thermal derating and second breakdown derating.

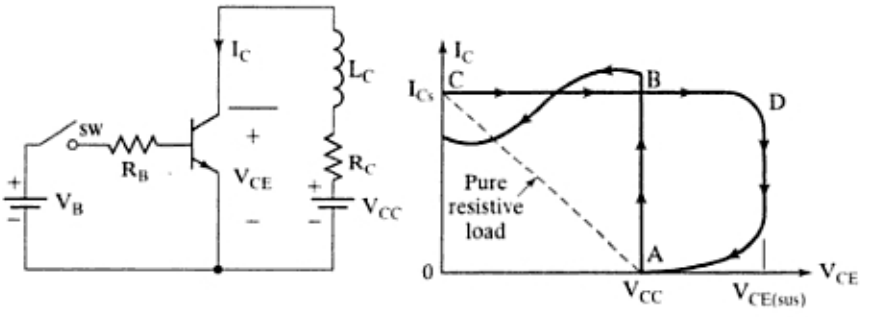
Breakdown voltages. A *breakdown voltage* is defined as the absolute maximum voltage between two terminals with the third terminal open, shorted, or biased in either forward or reverse direction. At breakdown the voltage remains relatively constant, where the current rises rapidly. The following breakdown voltages are quoted by the manufacturers:

V_{EBO}: the maximum voltage between the emitter terminal and base terminal with collector terminal open circuited.

V_{CEV} or V_{CEX}: the maximum voltage between the collector terminal and emitter terminal at a specified negative voltage applied between base and emitter.

$V_{CEO(SUS)}$: the maximum sustaining voltage between the collector terminal and emitter terminal with the base open circuited. This rating is specified at the maximum collector current and voltage, appearing simultaneously across the device with a specified value of load inductance.

Let us consider the circuit in Figure 4.14a. When the switch SW is closed, the collector current increases, and after a transient, the steady-state collector current is



(a) Test circuit (b) Load lines

FIGURE 4.14

Turn-on and turn-off load lines.

$I_{CS} = (V_{CC} - V_{CE(sat)})/R_C$. For an inductive load, the load line would be the path ABC shown in Figure 4.14b. If the switch is opened to remove the base current, the collector current begins to fall and a voltage of $L(di/dt)$ is induced across the inductor to oppose the current reduction. The transistor is subjected to a transient voltage. If this voltage reaches the sustaining voltage level, the collector voltage remains approximately constant and the collector current falls. After a short time, the transistor is in the off-state and the turn-off load line is shown in Figure 4.14b by the path CDA.

Example 4.4 Finding the Case Temperature of a BJT

The maximum junction temperature of a transistor is $T_J = 150°C$ and the ambient temperature is $T_A = 25°C$. If the thermal impedances are $R_{JC} = 0.4°C/W$, $R_{CS} = 0.1°C/W$, and $R_{SA} = 0.5°C/W$, calculate (a) the maximum power dissipation, and (b) the case temperature.

Solution

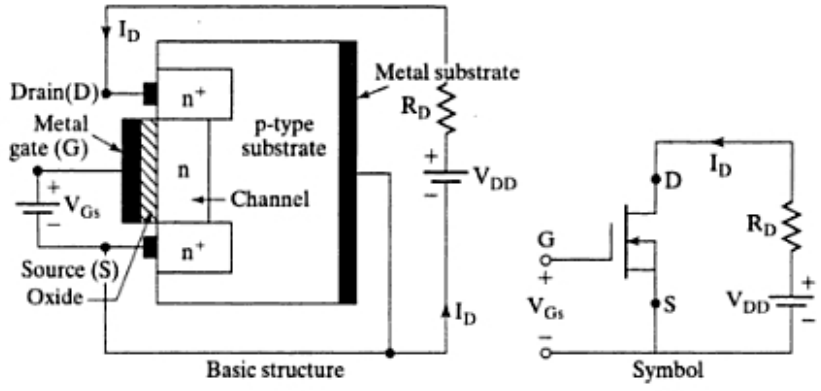
a. $T_J - T_A = P_T(R_{JC} + R_{CS} + R_{SA}) = P_T R_{JA}$, $R_{JA} = 0.4 + 0.1 + 0.5 = 1.0$, and $150 - 25 = 1.0P_T$, which gives the maximum power dissipation as $P_T = 125$ W.

b. $T_C = T_J - P_T R_{JC} = 150 - 125 \times 0.4 = 100°C$.

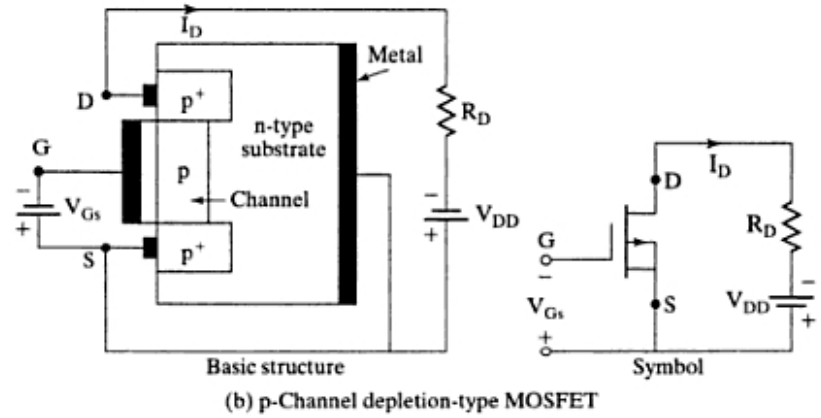
4.3 POWER MOSFETs

A BJT is a current-controlled device and requires base current for current flow in the collector. Because the collector current is dependent on the input (or base) current, the current gain is highly dependent on the junction temperature.

A power MOSFET is a voltage-controlled device and requires only a small input current. The switching speed is very high and the switching times are of the order of nanoseconds. Power MOSFETs find increasing applications in low-power high-frequency converters. MOSFETs do not have the problems of second breakdown phenomena as do BJTs. However, MOSFETs have the problems of electrostatic discharge and require special care in handling. In addition, it is relatively difficult to protect them under short-circuited fault conditions.



(a) n-Channel depletion-type MOSFET



(b) p-Channel depletion-type MOSFET

FIGURE 4.15
Depletion-type MOSFETs.

The two types of MOSFETs are (1) depletion MOSFETs, and (2) enhancement MOSFETs [6–8]. An *n*-channel depletion-type MOSFET is formed on a *p*-type silicon substrate as shown in Figure 4.15a, with two heavily doped n^+ silicon for low-resistance connections. The gate is isolated from the channel by a thin oxide layer. The three terminals are called *gate, drain*, and *source*. The substrate is normally connected to the source. The gate-to-source voltage V_{GS} could be either positive or negative. If V_{GS} is negative, some of the electrons in the *n*-channel area are repelled and a depletion region is created below the oxide layer, resulting in a narrower effective channel and a high resistance from the drain to source R_{DS}. If V_{GS} is made negative enough, the channel becomes completely depleted, offering a high value of R_{DS}, and no current flows from the drain to source, $I_{DS} = 0$. The value of V_{GS} when this happens is called *pinch-off voltage* V_P. On the other hand, V_{GS} is made positive, the channel becomes wider, and I_{DS} increases due to reduction in R_{DS}. With a *p*-channel depletion-type MOSFET, the polarities of V_{DS}, I_{DS}, and V_{GS} are reversed as shown in Figure 4.15b.

An *n*-channel enhancement-type MOSFET has no physical channel, as shown in Figure 4.16a. If V_{GS} is positive, an induced voltage attracts the electrons from the

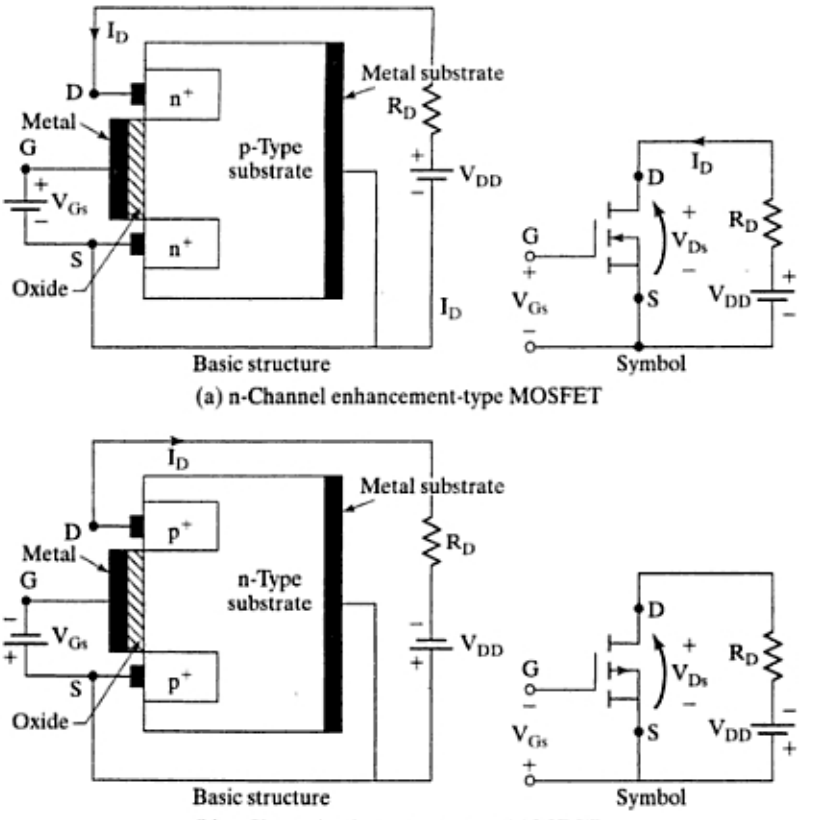


FIGURE 4.16

Enhancement-type MOSFETs.

p-substrate and accumulate them at the surface beneath the oxide layer. If V_{GS} is greater than or equal to a value known as *threshold voltage* V_T, a sufficient number of electrons are accumulated to form a virtual *n*-channel and the current flows from the drain to source. The polarities of V_{DS}, I_{DS}, and V_{GS} are reversed for a *p*-channel enhancement-type MOSFET as shown in Figure 4.16b. Power MOSFETs of various sizes are shown in Figure 4.17.

Because a depletion MOSFET remains on at zero gate voltage whereas an enhancement type MOSFET remains off at zero gate voltage, the enhancement type MOSFETS are generally used as switching devices in power electronics. The cross section of a power MOSFET known as a vertical (V) MOSFET is shown in Figure 4.18a.

When the gate has a sufficiently positive voltage with respect to the source, the effect of its electric field pulls electrons from the $n+$ layer into the p layer. This opens a channel closest to the gate, which in turn allows the current to flow from the drain to the source. There is a silicon oxide (SiO) dielectric layer between the gate metal and the $n+$ and p junction. MOSFET is heavily doped on the drain side to create an $n+$ buffer below the n-drift layer. This buffer prevents the depletion layer from reaching

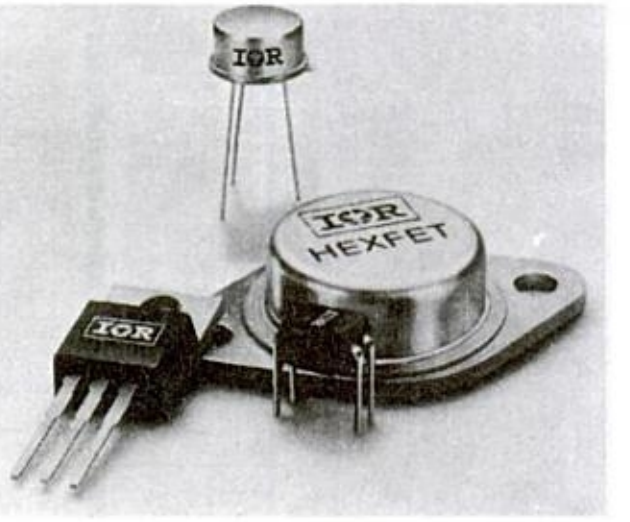
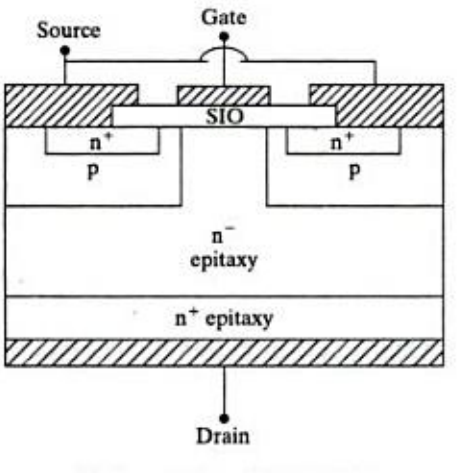


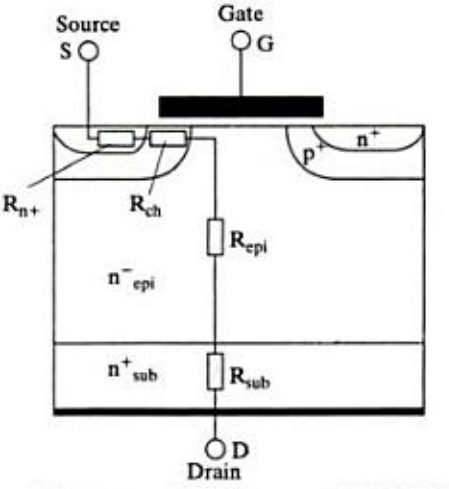
FIGURE 4.17
Power MOSFETs. (Courtesy of International Rectifier.)

the metal, evens out the voltage stress across the n layer, and also reduces the forward voltage drop during conduction. The buffer layer also makes it an asymmetric device with rather low reverse voltage capability.

MOSFETs require low gate energy, and have a very fast switching speed and low switching losses. The input resistance is very high, 10^9 to 10^{11} Ω. MOSFETs, however, suffer from the disadvantage of high forward on-state resistance as shown in Figure 4.18b, and hence high on-state losses, which makes them less attractive as power devices, but they are excellent as gate amplifying devices for thyristors (see Chapter 7).



(a) Cross section of V-MOSFET



(b) On-state series resistances of V-MOSFET

FIGURE 4.18
Cross sections of MOSFETs. [Ref. 10, G. Deboy]

4.3.1 Steady-State Characteristics

The MOSFETs are voltage-controlled devices and have a very high input impedance. The gate draws a very small leakage current, on the order of nanoamperes. The current gain, which is the ratio of drain current I_D, to input gate current I_G, is typically on the order of 10^9. However, the current gain is not an important parameter. The *transconductance*, which is the ratio of drain current to gate voltage, defines the transfer characteristics and is a very important parameter.

The transfer characteristics of *n*-channel and *p*-channel MOSFETs are shown in Figure 4.19. Figure 4.20 shows the output characteristics of an *n*-channel enhancement MOSFET. There are three regions of operation: (1) cutoff region, where $V_{GS} \leq V_T$; (2) pinch-off or saturation region, where $V_{DS} \geq V_{GS} - V_T$; and (3) linear region, where $V_{DS} \leq V_{GS} - V_T$. The pinch-off occurs at $V_{DS} = V_{GS} - V_T$. In the linear region, the drain current I_D varies in proportion to the drain–source voltage V_{DS}. Due to high drain current and low drain voltage, the power MOSFETs are operated in the linear region for switching actions. In the saturation region, the drain current remains almost constant for any increase in the value of V_{DS} and the transistors are used in this region for voltage amplification. It should be noted that saturation has the opposite meaning to that for bipolar transistors.

The steady-state model, which is the same for both depletion-type and enhancement-type MOSFETs, is shown in Figure 4.21. The transconductance g_m is defined as

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}=\text{constant}} \tag{4.37}$$

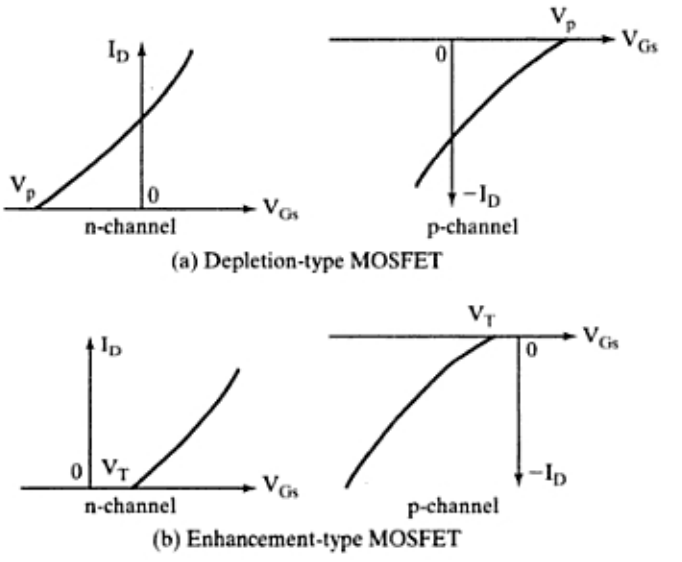


FIGURE 4.19
Transfer characteristics of MOSFETs.

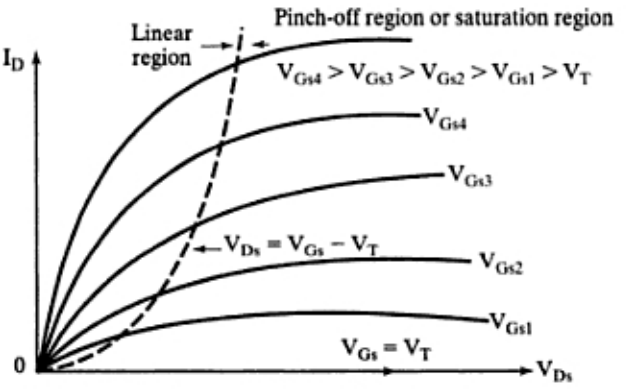


FIGURE 4.20
Output characteristics of enhancement-type MOSFET.

The output resistance, $r_o = R_{DS}$, which is defined as

$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D} \tag{4.38}$$

is normally very high in the pinch-off region, typically on the order of megohms and is very small in the linear region, typically on the order of milliohms.

For the depletion-type MOSFETs, the gate (or input) voltage could be either positive or negative. However, the enhancement-type MOSFETs respond to a positive gate voltage only. The power MOSFETs are generally of the enhancement type. However, depletion-type MOSFETs would be advantageous and simplify the logic design in some applications that require some form of logic-compatible dc or ac switch that would remain on when the logic supply falls and V_{GS} becomes zero. The characteristics of depletion-type MOSFETs are not discussed further.

4.3.2 Switching Characteristics

Without any gate signal, an enhancement-type MOSFET may be considered as two diodes connected back to back or as an *NPN*-transistor. The gate structure has parasitic

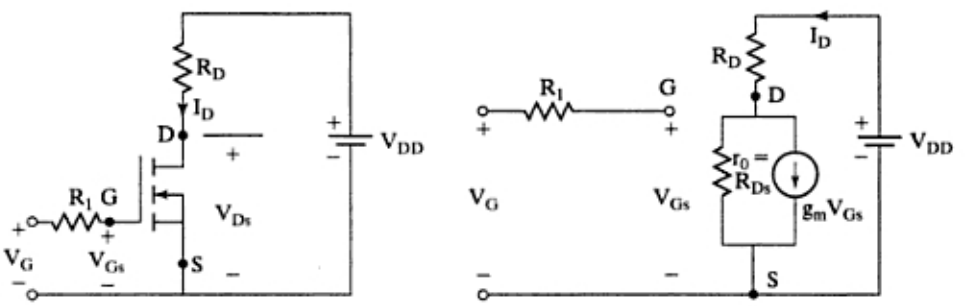


FIGURE 4.21
Steady-state switching model of MOSFETs.

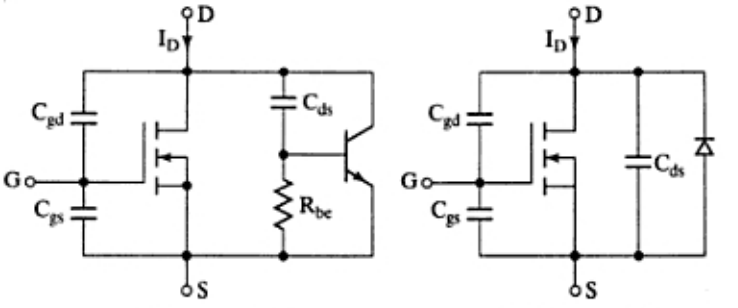


FIGURE 4.22

Parasitic model of enhancement of MOSFETs.

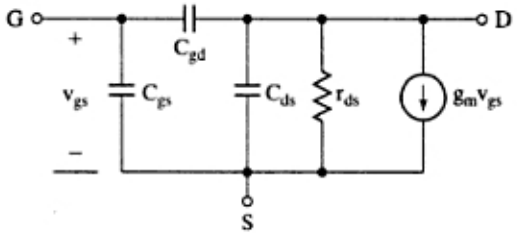


FIGURE 4.23

Switching model of MOSFETs.

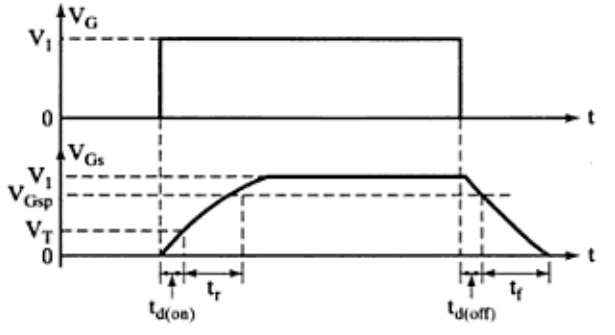


FIGURE 4.24

Switching waveforms and times.

capacitances to the source, C_{gs}, and to the drain, C_{gd}. The *npn*-transistor has a reverse-bias junction from the drain to the source and offers a capacitance, C_{ds}. Figure 4.22a shows the equivalent circuit of a parasitic bipolar transistor in parallel with a MOSFET. The base-to-emitter region of an *NPN*-transistor is shorted at the chip by metalizing the source terminal and the resistance from the base to emitter due to bulk resistance of *n*- and *p*-regions, R_{be}, is small. Hence, as MOSFET may be considered as having an internal diode and the equivalent circuit is shown in Figure 4.22b. The parasitic capacitances are dependent on their respective voltages.

The switching model of MOSFETs is shown in Figure 4.23. The typical switching waveforms and times are shown in Figure 4.24. The *turn-on delay* $t_{d(on)}$ is the

time that is required to charge the input capacitance to threshold voltage level. The *rise time* t_r is the gate-charging time from the threshold level to the full-gate voltage V_{GSP}, which is required to drive the transistor into the linear region. The *turn-off delay time* $t_{d(off)}$ is the time required for the input capacitance to discharge from the overdrive gate voltage V_1 to the pinch-off region. V_{GS} must decrease significantly before V_{DS} begins to rise. The *fall time* t_f is the time that is required for the input capacitance to discharge from the pinch-off region to threshold voltage. If $V_{GS} \leq V_T$, the transistor turns off.

4.4 COOLMOS

COOLMOS [9–11], which is a new technology for high voltage power MOSFETs, implements a compensation structure in the vertical drift region of a MOSFET to improve the on-state resistance. It has a lower on-state resistance for the same package compared with that of other MOSFETs. The conduction losses are at least five times less as compared with those of the conventional MOSFET technology. It is capable of handling two to three times more output power as compared with that of the conventional MOSFET in the same package. The active chip area of COOLMOS is approximately five times smaller than that of a standard MOSFET.

Figure 4.25 shows the cross section of a COOLMOS. The device enhances the doping of the current conducting *n*-doped layer by roughly one order of magnitude without altering the blocking capability of the device. A high-blocking voltage V_{BR} of

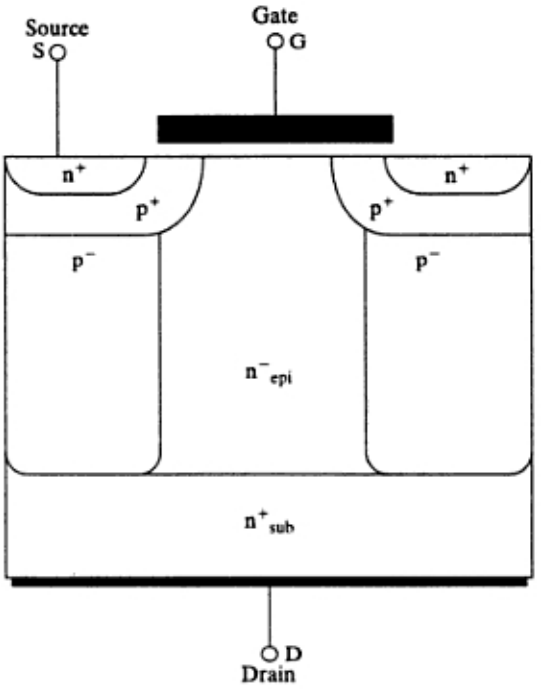


FIGURE 4.25
Cross section of COOLMOS.

the transistor requires a relative thick and low-doped epitaxial layer leading to the well-known law [12] that relates the drain to source resistance to V_{BR} by

$$R_{D(\text{on})} = V_{BR}^{k_c} \tag{4.39}$$

where k_c is a constant between 2.4 and 2.6.

This limitation is overcome by adding columns of the opposite doping type that are implemented into the drift region in a way that the doping integral along a line perpendicular to the current flow remains smaller than the material specific breakthrough charge, which for silicon is about 2×10^{12} cm^{-2}. This concept requires a compensation of the additional charge in the n region by adjacently situated p-doped regions. These charges create a lateral electric field, which does not contribute to the vertical field profile. In other words, the doping concentration is integrated along a line perpendicular to the interface created by the p- and n-regions.

Majority carriers provide the electrical conductivity only. Because there is no bipolar current contribution, the switching losses are equal to that of conventional MOSFETs. The doping of the voltage sustaining the layer is raised by roughly one order of magnitude; additional vertical p-stripes, which are inserted into the structure compensate for the surplus current conducting n-charge. The electric field inside the structure is fixed by the net charge of the two opposite doped columns. Thus, a nearly horizontal field distribution can be achieved if both regions counterbalance each other perfectly. The fabrication of adjacent pairs of p- and n-doped regions with practically zero net charge requires a precision manufacturing. Any charge imbalance impacts the blocking voltage of the device. For higher blocking voltages only the depth of the columns has to be increased without the necessity to alter the doping. This leads to a linear relationship [10] between blocking voltage and on-resistance as shown in Figure 4.26. The on-state resistance of a 600-V, 47-A COOLMOS is 70 mΩ. The COOLMOS has a linear v–i characteristic with a low-threshold voltage [10].

The COOLMOS devices can be used in applications up to power range of 2 kVA such as power supplies for workstations and server, uninterruptible power supplies (UPS), high-voltage converters for microwave and medical systems, induction ovens, and welding equipment. These devices can replace conventional power MOSFETs in all applications in most cases without any circuit adaptation. At switching frequencies above 100 kHz, COOLMOS devices offer a superior current-handling capability such as smallest required chip area at a given current. The devices have the advantage of an intrinsic inverse diode. Any parasitic oscillations, which could cause negative undershoots of the drain-source voltage, are clamped by the diode to a defined value.

4.5 SITs

An SIT is a high-power, high-frequency device. Since the invention of the static induction devices in Japan by J. Nishizawa [17], the number of devices in this family is growing [19]. It is essentially the solid-state version of the triode vacuum tube. The silicon cross section of an SIT [15] and its symbol are shown in Figure 4.27. It is a vertical structure device with short multichannels. Thus, it is not subject to area limitation and is suitable for high-speed, high-power operation. The gate electrodes are buried within the drain and source n-epi layers. An SIT is identical to a JFET except for vertical and buried gate construction,

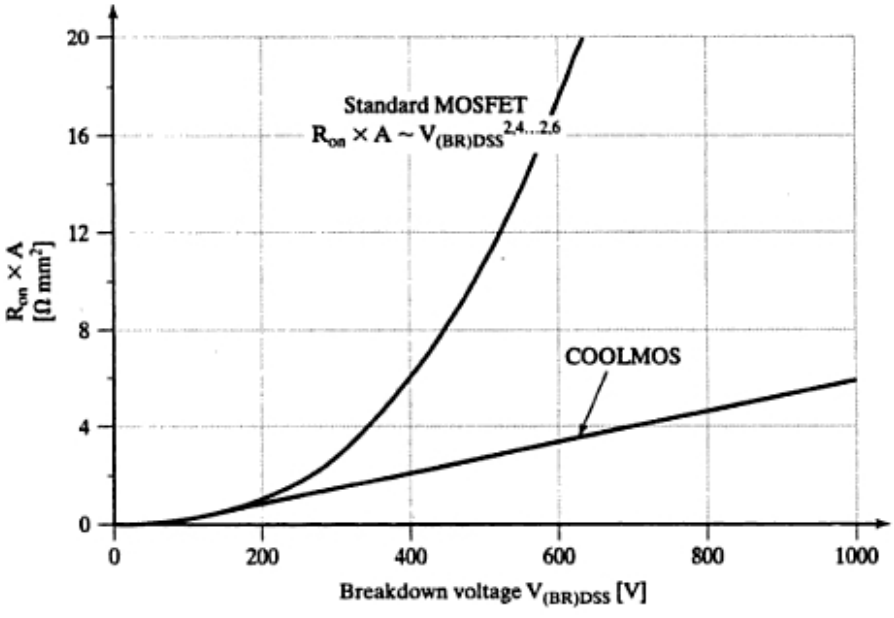


FIGURE 4.26

The linear relationship between blocking voltage and on-resistance. [Ref. 10, G. Deboy]

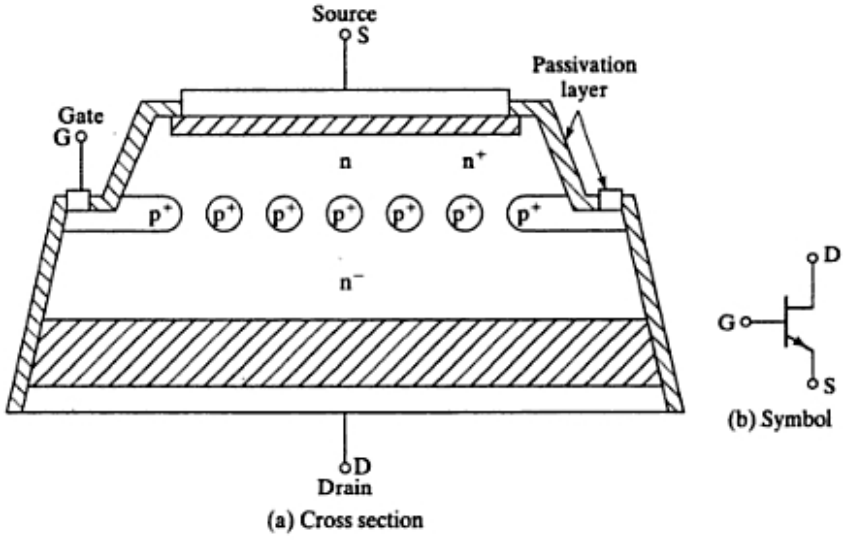


FIGURE 4.27

Cross section and symbol for SITs.

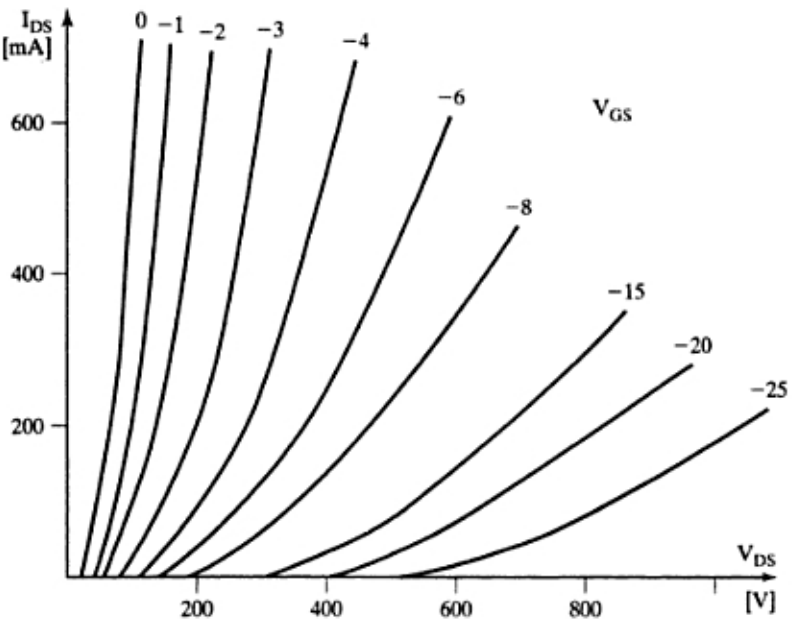


FIGURE 4.28

Typical characteristics of SITs. [Ref. 18, 19]

which gives a lower channel resistance, causing a lower drop. An SIT has a short channel length, low gate series resistance, low gate–source capacitance, and small thermal resistance. It has a low noise, low distortion, and high audiofrequency power capability. The turn-on and turn-off times are very small, typically 0.25 μs.

The on-state drop is high, typically 90 V for a 180-A device and 18 V for an 18-A device. An SIT normally is an on device, and a negative gate voltage holds it off. The normally on-characteristic and the high on-state drop limit its applications for general power conversions. The typical characteristics of SITs are shown in Figure 4.28 [18]. An electrostatically induced potential barrier controls the current in static induction devices. The SITs can operate with the power of 100 KVA at 100 kHz or 10 VA at 10 GHz. The current rating of SITs can be up to 1200 V, 300 A, and the switching speed can be as high as 100 kHz. It is most suitable for high-power, high-frequency applications (e.g., audio, VHF/UHF, and microwave amplifiers).

4.6 IGBTs

An IGBT combines the advantages of BJTs and MOSFETs. An IGBT has high input impedance, like MOSFETs, and low on-state conduction losses, like BJTs. However, there is no second breakdown problem, as with BJTs. By chip design and structure, the equivalent drain-to-source resistance R_{DS} is controlled to behave like that of a BJT [13–14].

The silicon cross section of an IGBT is shown in Figure 4.29a, which is identical to that of an MOSFET except the p^+ substrate. However, the performance of an IGBT is

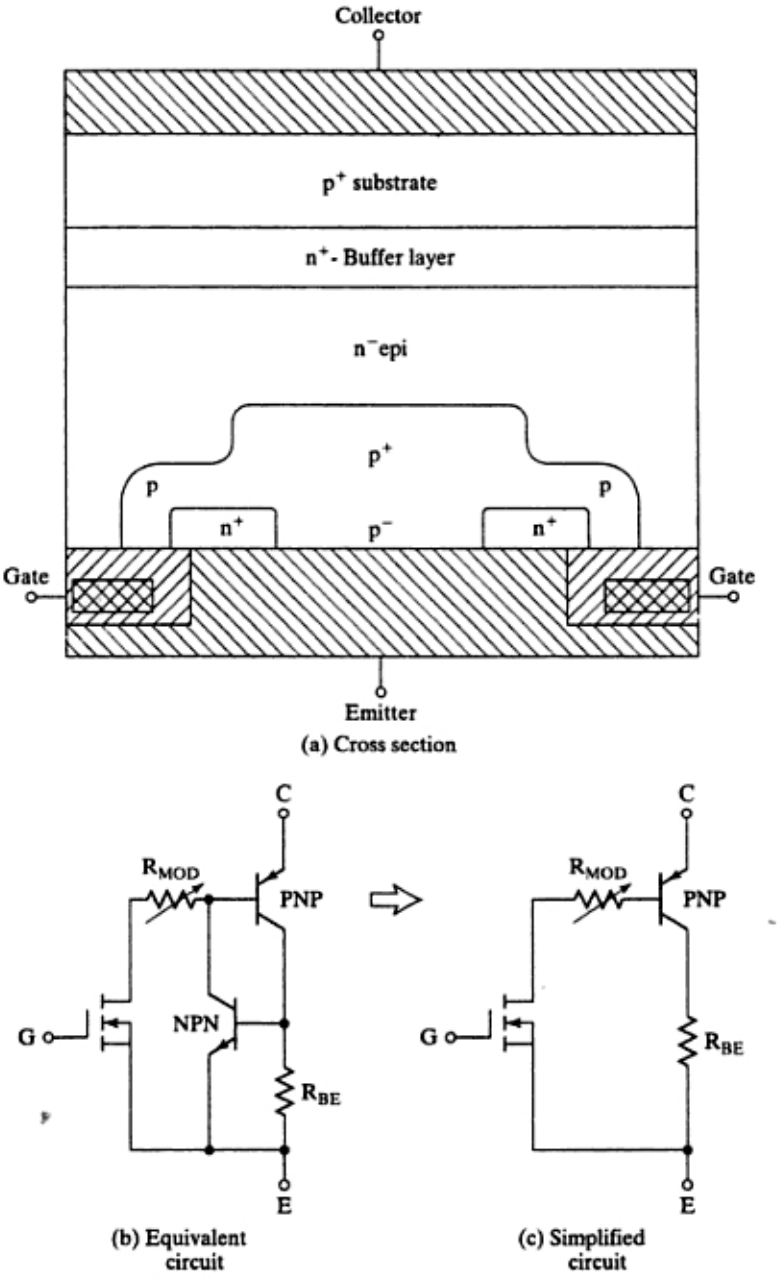


FIGURE 4.29

Cross section and equivalent circuit for IGBTs.

closer to that of a BJT than an MOSFET. This is due to the p^+ substrate, which is responsible for the minority carrier injection into the n-region. The equivalent circuit is shown in Figure 4.29b, which can be simplified to Figure 4.29c. An IGBT is made of four alternate *PNPN* layers, and could latch like a thyristor given the necessary

condition: $(\alpha_{npn} + \alpha_{pnp}) > 1$. The n^+-buffer layer and the wide epi base reduce the gain of the *NPN*-terminal by internal design, thereby avoiding latching. IGBTs have two structures of IGBTs: punch-through (PT) and nonpunch through (NPT). In the PT IGBT structure, the switching time is reduced by use of a heavily doped *n*-buffer layer in the drift region near the collector. In the NPT structure, carrier lifetime is kept more than that of a PT structure, which causes conductivity modulation of the drift region and reduces the on-state voltage drop. An IGBT is a voltage-controlled device similar to a power MOSFET. Like an MOSFET, when the gate is made positive with respect to the emitter for turn-on, *n* carriers are drawn into the *p*-channel near the gate region; this results in a forward bias of the base of the *npn*-transistor, which thereby turns on. An IGBT is turned on by just applying a positive gate voltage to open the channel for *n* carriers and is turned off by removing the gate voltage to close the channel. It requires a very simple driver circuit. It has lower switching and conducting losses while sharing many of the appealing features of power MOSFETS, such as ease of gate drive, peak current, capability, and ruggedness. An IGBT is inherently faster than a BJT. However, the switching speed of IGBTs is inferior to that of MOSFETs.

The symbol and circuit of an IGBT switch are shown in Figure 4.30. The three terminals are gate, collector, and emitter instead of gate, drain, and source for an MOSFET. The typical output characteristics of i_C versus v_{CE} are shown in Figure 4.31a for various gate–emitter voltage v_{GE}. The typical transfer characteristic of i_C versus v_{GE} is

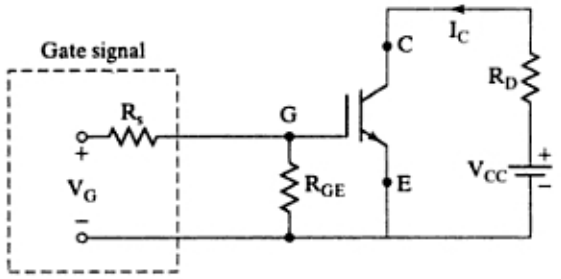


FIGURE 4.30

Symbol and circuit for an IGBT.

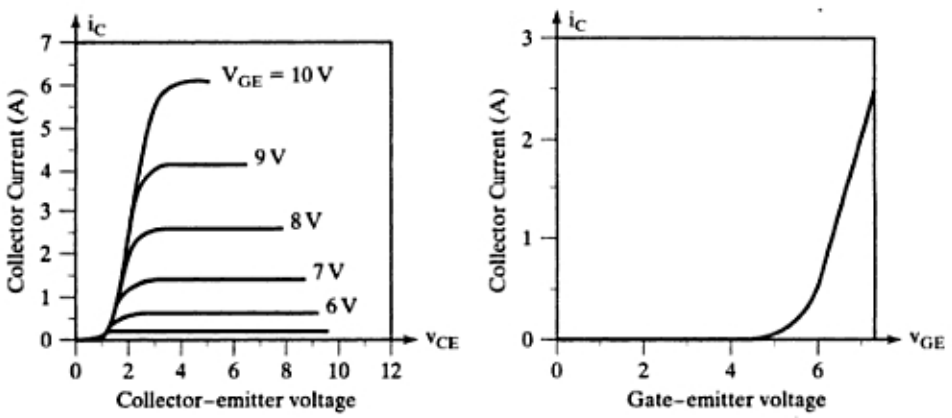


FIGURE 4.31

Typical output and transfer characteristics of IGBTs.

shown in Figure 4.31b. The parameters and their symbols are similar to that of MOSFETs, except that the subscripts for source and drain are changed to emitter and collector, respectively. The current rating of a single IGBT can be up to 1200 V, 400 A, and the switching frequency can be up to 20 kHz. IBGTs are finding increasing applications in medium-power applications such as dc and ac motor drives, power supplies, solid-state relays, and contractors.

As the upper limits of commercially available IGBT ratings are increasing (e.g., as high as 6500 V and 2400 A), IGBTs are finding and replacing applications where BJTs and conventional MOSFETs were predominantly used as switches.

4.7 SERIES AND PARALLEL OPERATION

Transistors may be operated in series to increase their voltage-handling capability. It is very important that the series-connected transistors are turned on and off simultaneously. Otherwise, the slowest device at turn-on and the fastest device at turn-off may be subjected to the full voltage of the collector–emitter (or drain–source) circuit and that particular device may be destroyed due to a high voltage. The devices should be matched for gain, transconductance, threshold voltage, on-state voltage, turn-on time, and turn-off time. Even the gate or base drive characteristics should be identical. Voltage-sharing networks similar to diodes could be used.

Transistors are connected in parallel if one device cannot handle the load current demand. For equal current sharings, the transistors should be matched for gain, transconductance, saturation voltage, and turn-on time and turn-off time. In practice, it is not always possible to meet these requirements. A reasonable amount of current sharing (45 to 55% with two transistors) can be obtained by connecting resistors in series with the emitter (or source) terminals, as shown in Figure 4.32.

The resistors in Figure 4.32 help current sharing under steady-state conditions. Current sharing under dynamic conditions can be accomplished by connecting coupled inductors as shown in Figure 4.33. If the current through Q_1 rises, the $L(di/dt)$ across L_1 increases, and a corresponding voltage of opposite polarity is induced across inductor L_2. The result is a low-impedance path, and the current is shifted to Q_2. The inductors would generate voltage spikes and they may be expensive and bulky, especially at high currents.

BJTs have a negative temperature coefficient. During current sharing, if one BJT carries more current, its on-state resistance decreases and its current increases further, whereas MOSFETs have a positive temperature coefficient and parallel operation is

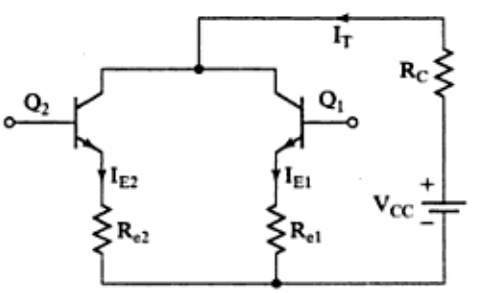


FIGURE 4.32
Parallel connection of transistors.

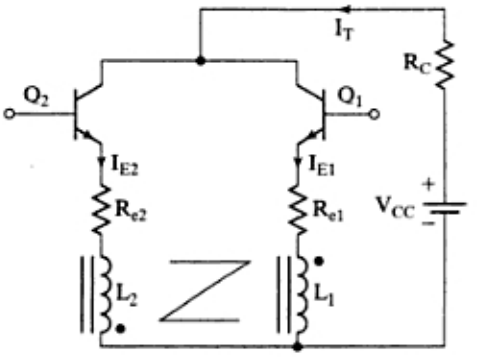


FIGURE 4.33
Dynamic current sharing.

relatively easy. The MOSFET that initially draws higher current heats up faster and its on-state resistance increases, resulting in current shifting to the other devices. IGBTs require special care to match the characteristics due to the variations of the temperature coefficients with the collector current.

Example 4.5 Finding the Current Sharing by Two Parallel MOSFETs

Two MOSFETs that are connected in parallel similar to Figure 4.32 carry a total current of $I_T = 20$ A. The drain-to-source voltage of MOSFET M_1 is $V_{DS1} = 2.5$ V and that of MOSFET M_2 is $V_{DS2} = 3$ V. Determine the drain current of each transistor and difference in current sharing if the current sharing series resistances are (a) $R_{s1} = 0.3\ \Omega$ and $R_{s2} = 0.2\ \Omega$, and (b) $R_{s1} = R_{s2} = 0.5\ \Omega$.

Solution

a. $I_{D1} + I_{D2} = I_T$ and $V_{DS1} + I_{D1}R_{S1} = V_{DS2} + I_{D2}R_{S2} = V_{DS2} = R_{S2}(I_T - I_{D1})$.

$$\begin{aligned} SI_{D1} &= \frac{V_{DS2} - V_{DS1} + I_T R_{s2}}{R_{s1} + R_{s2}} \\ &= \frac{3 - 2.5 + 20 \times 0.2}{0.3 + 0.2} = 9\ \text{A} \quad \text{or} \quad 45\% \\ I_{D2} &= 20 - 9 = 11\ \text{A} \quad \text{or} \quad 55\% \\ \Delta I &= 55 - 45 = 10\% \end{aligned} \tag{4.40}$$

b. $I_{D1} = \dfrac{3 - 2.5 + 20 \times 0.5}{0.5 + 0.5} = 10.5\ \text{A} \quad \text{or} \quad 52.5\%$

$I_{D2} = 20 - 10.5 = 9.5\ \text{A} \quad \text{or} \quad 47.5\%$

$\Delta I = 52.5 - 47.5 = 5\%$

4.8 *di/dt* AND *dv/dt* LIMITATIONS

Transistors require certain turn-on and turn-off times. Neglecting the delay time t_d and the storage time t_s, the typical voltage and current waveforms of a BJT switch are

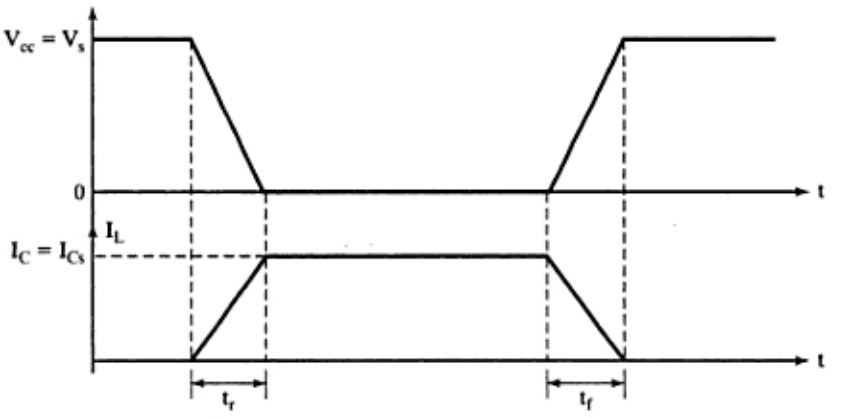


FIGURE 4.34
Voltage and current waveforms.

shown in Figure 4.34. During turn-on, the collector current rises and the *di/dt* is

$$\frac{di}{dt} = \frac{I_L}{t_r} = \frac{I_{cs}}{t_r} \tag{4.41}$$

During turn-off, the collector–emitter voltage must rise in relation to the fall of the collector current, and *dv/dt* is

$$\frac{dv}{dt} = \frac{V_s}{t_f} = \frac{V_{cs}}{t_f} \tag{4.42}$$

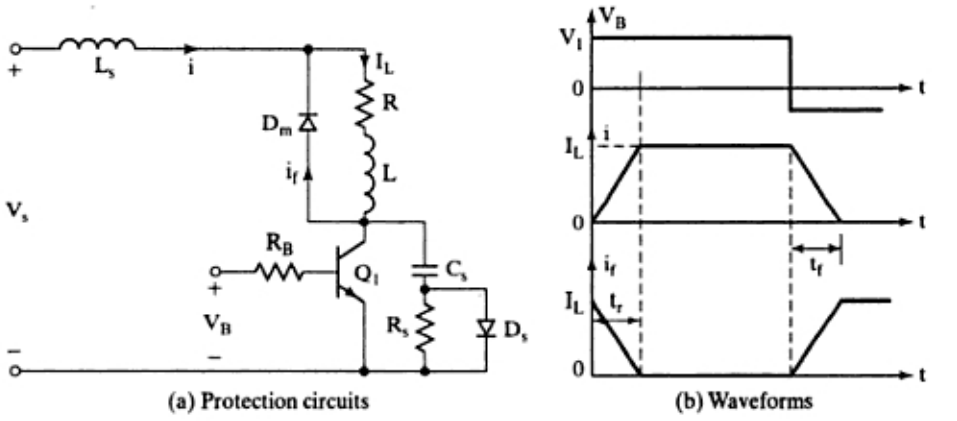
The conditions *di/dt* and *dv/dt* in Eqs. (4.41) and (4.42) are set by the transistor switching characteristics and must be satisfied during turn-on and turn-off. Protection circuits are normally required to keep the operating *di/dt* and *dv/dt* within the allowable limits of the transistor. A typical transistor switch with *di/dt* and *dv/dt* protection is shown in Figure 4.35a, with the operating waveforms in Figure 4.35b. The *RC* network across the transistor is known as the *snubber circuit*, or *snubber*, and limits the *dv/dt*. The inductor L_s, which limits the *di/dt*, is sometimes called a *series snubber*.

Let us assume that under steady-state conditions the load current I_L is freewheeling through diode D_m, which has negligible reverse recovery time. When transistor Q_1 is turned on, the collector current rises and current of diode D_m falls, because D_m behaves as short-circuited. The equivalent circuit during turn-on is shown in Figure 4.36a and turn-on *di/dt* is

$$\frac{di}{dt} = \frac{V_s}{L_s} \tag{4.43}$$

Equating Eq. (4.41) to Eq. (4.43) gives the value of L_s,

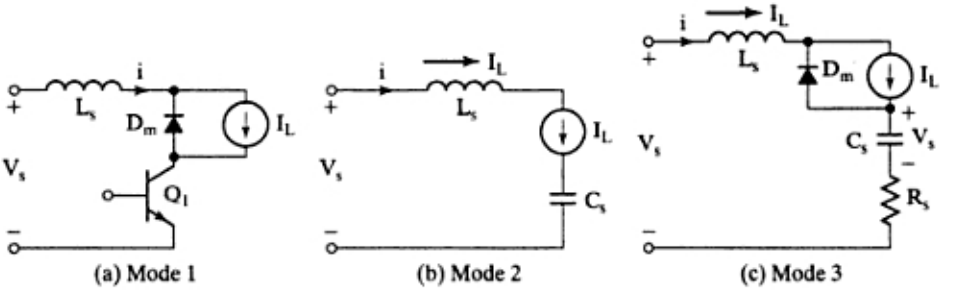
$$L_s = \frac{V_s t_r}{I_L} \tag{4.44}$$



(a) Protection circuits (b) Waveforms

FIGURE 4.35

Transistor switch with *di/dt* and *dv/dt* protection.



(a) Mode 1 (b) Mode 2 (c) Mode 3

FIGURE 4.36

Equivalent circuits.

During turn-off, the capacitor C_s charges by the load current and the equivalent circuit is shown in Figure 4.36b. The capacitor voltage appears across the transistor and the *dv/dt* is

$$\frac{dv}{dt} = \frac{I_L}{C_s} \tag{4.45}$$

Equating Eq. (4.42) to Eq. (4.45) gives the required value of capacitance,

$$C_s = \frac{I_L t_f}{V_s} \tag{4.46}$$

Once the capacitor is charged to V_s, the freewheeling diode turns on. Due to the energy stored in L_s, there is a damped resonant circuit as shown in Figure 4.36c. The transient analysis of *RLC* circuit is discussed in Section 16.4. The *RLC* circuit is normally

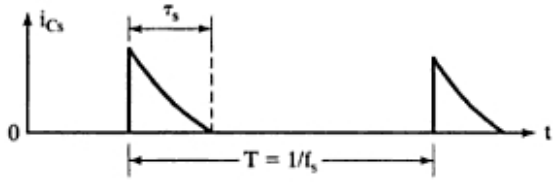


FIGURE 4.37
Discharge current of snubber capacitor.

made critically damped to avoid oscillations. For unity critical damping, $\delta = 1$, and Eq. (18.11) yields

$$R_s = 2\sqrt{\frac{L_s}{C_s}} \tag{4.47}$$

The capacitor C_s has to discharge through the transistor and this increases the peak current rating of the transistor. The discharge through the transistor can be avoided by placing resistor R_s across C_s instead of placing R_s across D_s.

The discharge current is shown in Figure 4.37. When choosing the value of R_s, the discharge time, $R_sC_s = \tau_s$ should also be considered. A discharge time of one-third the switching period T_s is usually adequate.

$$3R_sC_s = T_s = \frac{1}{f_s}$$

or

$$R_s = \frac{1}{3f_sC_s} \tag{4.48}$$

Example 4.6 Finding the Snubber Values for Limiting *dv/dt* and *di/dt* Values of a BJT Switch

A bipolar transistor is operated as a chopper switch at a frequency of $f_s = 10$ kHz. The circuit arrangement is shown in Figure 4.35a. The dc voltage of the chopper is $V_s = 220$ V and the load current is $I_L = 100$ A. $V_{CE(sat)} = 0$ V. The switching times are $t_d = 0$, $t_r = 3$ μs, and $t_f = 1.2$ μs. Determine the values of (a) L_s; (b) C_s; (c) R_s for critically damped condition; (d) R_s, if the discharge time is limited to one-third of switching period; (e) R_s, if the peak discharge current is limited to 10% of load current; and (f) power loss due to RC snubber P_s, neglecting the effect of inductor L_s on the voltage of the snubber capacitor C_s.

Solution

$I_L = 100$ A, $V_s = 220$ V, $f_s = 10$ kHz, $t_r = 3$ μs, and $t_f = 1.2$ μs.

a. From Eq. (4.44), $L_s = V_st_r/I_L = 220 \times 3/100 = 6.6$ μH.

b. From Eq. (4.46), $C_s = I_Lt_f/V_s = 100 \times 1.2/220 = 0.55$ μF.

c. From Eq. (4.47), $R_s = 2\sqrt{L_s/C_s} = 2\sqrt{6.6/0.55} = 6.93$ Ω.

d. From Eq. (4.48), $R_s = 1/(3f_sC_s) = 10^3/(3 \times 10 \times 0.55) = 60.6$ Ω.

e. $V_s/R_s = 0.1 \times I_L$ or $220/R_s = 0.1 \times 100$ or $R_s = 22$ Ω.

f. The snubber loss, neglecting the loss in diode D_s, is

$$P_s \cong 0.5C_sV_s^2f_s \tag{4.49}$$
$$= 0.5 \times 0.55 \times 10^{-6} \times 220^2 \times 10 \times 10^3 = 133.1 \text{ W}$$

4.9 SPICE MODELS

Due to the nonlinear behavior of power electronics circuits, the computer-aided simulation plays an important role in the design and analysis of power electronics circuits and systems. Device manufacturers often provide SPICE models for power devices.

4.9.1 BJT SPICE Model

The PSpice model, which is based on the integral charge-control model of Gummel and Poon [16], is shown in Figure 4.38a. The static (dc) model that is generated by PSpice is shown in Figure 4.38b. If certain parameters are not specified, PSpice assumes the simple model of Ebers–Moll as shown in Figure 4.38c.

The model statement for *NPN*-transistors has the general form

```
.MODEL QNAME NPN (P1=V1 P2=V2 P3=V3 . . . PN=VN)
```

and the general form for *PNP*-transistors is

```
.MODEL QNAME PNP (P1=V1 P2=V2 P3=V3 . . . PN=VN)
```

where QNAME is the name of the BJT model. *NPN* and *PNP* are the type symbols for *NPN*- and *PNP*-transistors, respectively. P1, P2, .. and V1, V2, ... are the parameters and their values, respectively. The parameters that affect the switching behavior of a BJT in power electronics are IS, BF, CJE, CJC, TR, TF. The symbol for a BJT is Q, and its name must start with Q. The general form is

```
Q <name> NC NB NE NS QNAME [(area) value]
```

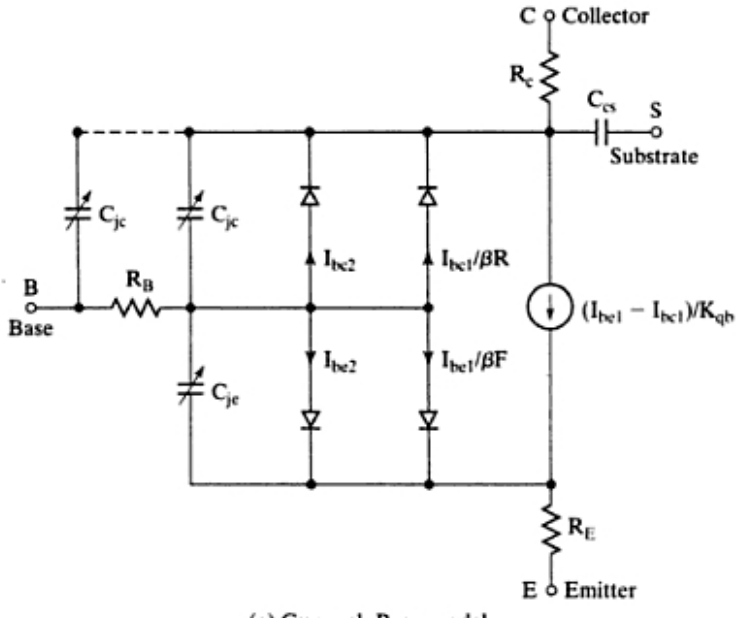
where NC, NB, NE, and NS are the collector, base, emitter, and substrate nodes, respectively. The substrate node is optional: If not specified, it defaults to ground. Positive current is the current that flows into a terminal. That is, the current flows from the collector node, through the device, to the emitter node for an *NPN*-BJT.

The parameters that significantly influence the switching behavior of a BJT are:

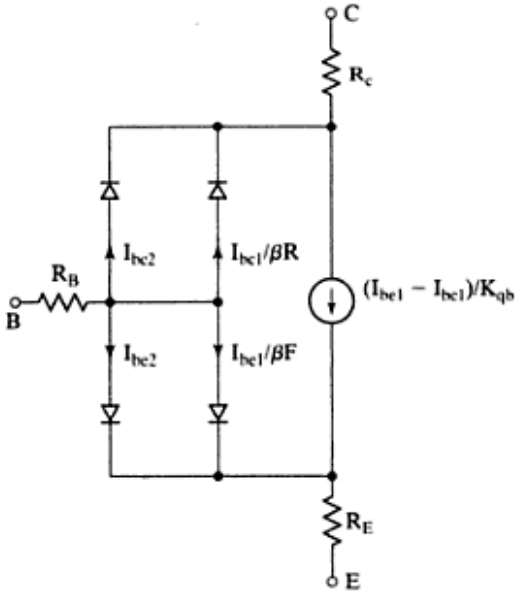
IS	P-N saturation current
BF	Ideal maximum forward beta
CJE	Base-emitter zero-bias *pn* capacitance
CJC	Base-collector zero-bias *pn* capacitance
TR	Ideal reverse transit time
TF	Ideal forward transit time

4.9.2 MOSFET SPICE Model

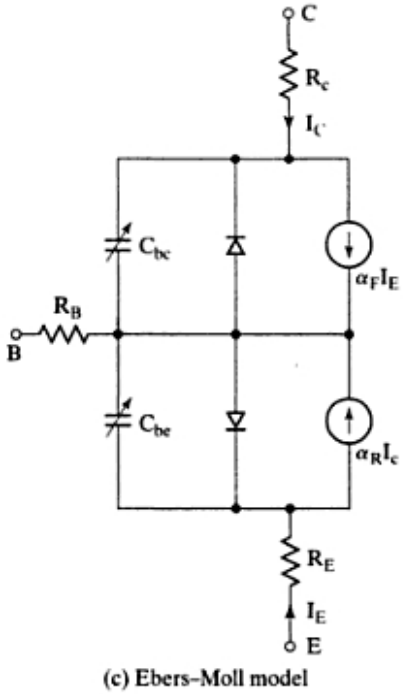
The PSpice model [16] of an *n*-channel MOSFET is shown in Figure 4.39a. The static (dc) model that is generated by PSpice is shown in Figure 4.39b. The model statement



(a) Gummel–Poon model



(b) Dc model



(c) Ebers–Moll model

FIGURE 4.38
PSpice BJT model

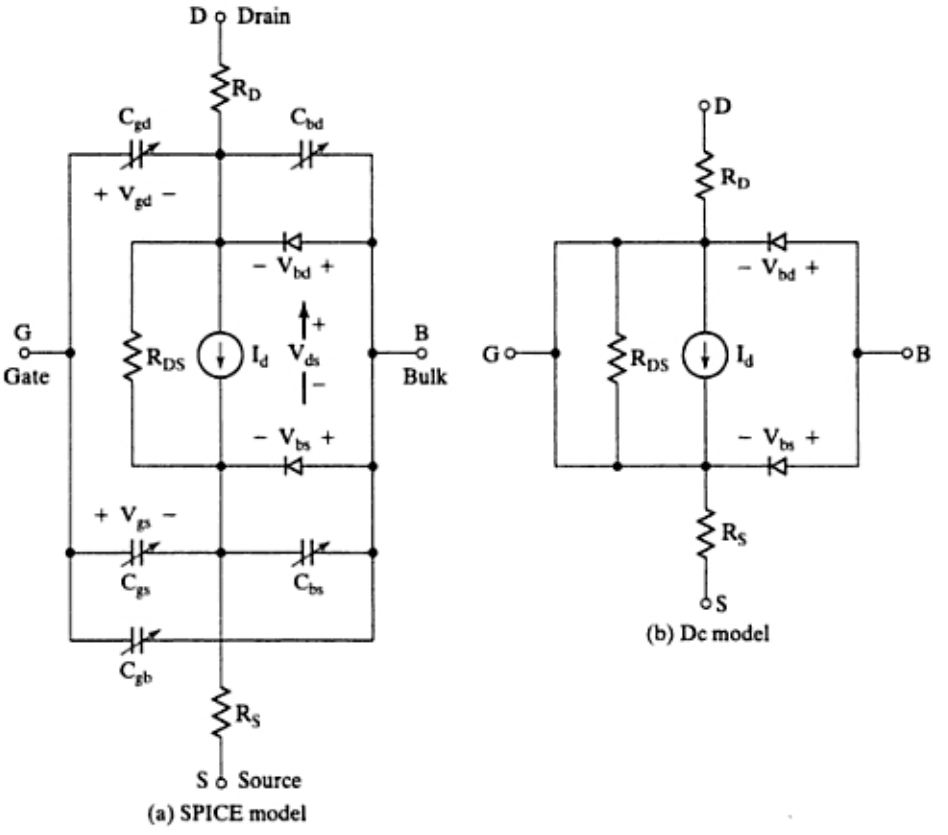


FIGURE 4.39

PSpice *n*-channel MOSFET model.

of *n*-channel MOSFETs has the general form

```
.MODEL MNAME NMOS (P1=V1 P2=V2 P3=V3 ... PN=VN)
```

and the statement for *p*-channel MOSFETs has the form

```
.MODEL MNAME PMOS (P1=V1 P2=V2 P3=V3 ... PN=VN)
```

where MNAME is the model name. NMOS and PMOS are the type symbols of *n*-channel and *p*-channel MOSFETs, respectively. The parameters that affect the switching behavior of an MOSFET in power electronics are L, W, VTO, KP, IS, CGSO, and CGDO.

The symbol for an MOSFET is M. The name of MOSFETs must start with M and it takes the general form

```
M<name>   ND    NG    NS    NB    MNAME
+         [L=<value>]   [W=<value>]
+         [AD=<value>]  [AS=<value>]
+         [PD=<value>]  [PS=<value>]
+         [NRD=<value>] [NRS=<value>]
+         [NRG=<value>] [NRB=<value>]
```

where ND, NG, NS, and NB are the drain, gate, source, and bulk (or substrate) nodes, respectively.

The parameters that significantly influence the switching behavior of an MOSFET are:

L	Channel length
W	Channel width
VTO	Zero-bias threshold voltage
IS	Bulk *pn*-saturation current
CGSO	Gate–source overlap capacitance and channel width
CGDO	Gate–drain overlap capacitance and channel width

For COOLMOS, SPICE does not support any models. However, the manufacturers provide models for COOLMOS [11].

4.9.3 IGBT SPICE Model

The *n*-channel IGBT consists of a *pnp*-bipolar transistor that is driven by an *n*-channel MOSFET. Therefore, the IGBT behavior is determined by physics of the bipolar and MOSFET devices. Several effects dominate the static and dynamic device characteristics. The internal circuit of an IGBT is shown in Figure 4.40a.

An IGBT circuit model [16], which relates the currents between terminal nodes as a nonlinear function of component variables and their rate of change, is shown in Figure 4.40b. The capacitance of the emitter–base junction C_{eb} is implicitly defined by the emitter–base voltage as a function of base charge. I_{ceb} is the emitter–base capacitor current that defines the rate of change of the base charge. The current through the collector–emitter redistribution capacitance I_{ccer} is part of the collector current, which in contrast to I_{css} depends on the rate of change of the base-emitter voltage. I_{bss} is part of the base current that does not flow through C_{eb} and does not depend on rate of change of base–collector voltage.

There are two main ways to model IGBT in SPICE: (1) composite model and (2) equation model. The composite model connects the existing SPICE *pnp*-BJT and *n*-channel MOSFET models. The equivalent circuit of the composite model is shown in Figure 4.41a. It connects the existing BIT and MOSFET models of PSpice in a Darlington configuration and uses the built-in equations of the two. The model computes quickly and reliably, but it does not model the behavior of the IGBT accurately.

The equation model [22, 23] implements the physics-based equations and models the internal carrier and charge to simulate the circuit behavior of the IGBT accurately. This model is complicated, often unreliable, and computationally slow because the equations are derived from the complex semiconductor physics theory. Simulation times can be over 10 times longer than those for the composite model.

There are numerous papers of SPICE modeling of IGBTs and Sheng [24] compares the merits and limitations of various models. Figure 4.41b shows the equivalent circuit of Sheng's model [21] that adds a current source from the drain to the gate. It has been found that the major inaccuracy in dynamic electrical properties is associated with the modeling of the drain to gate capacitance of the *n*-channel MOSFET. During high-voltage switching, the drain-to-gate capacitance C_{dg} changes by two orders of

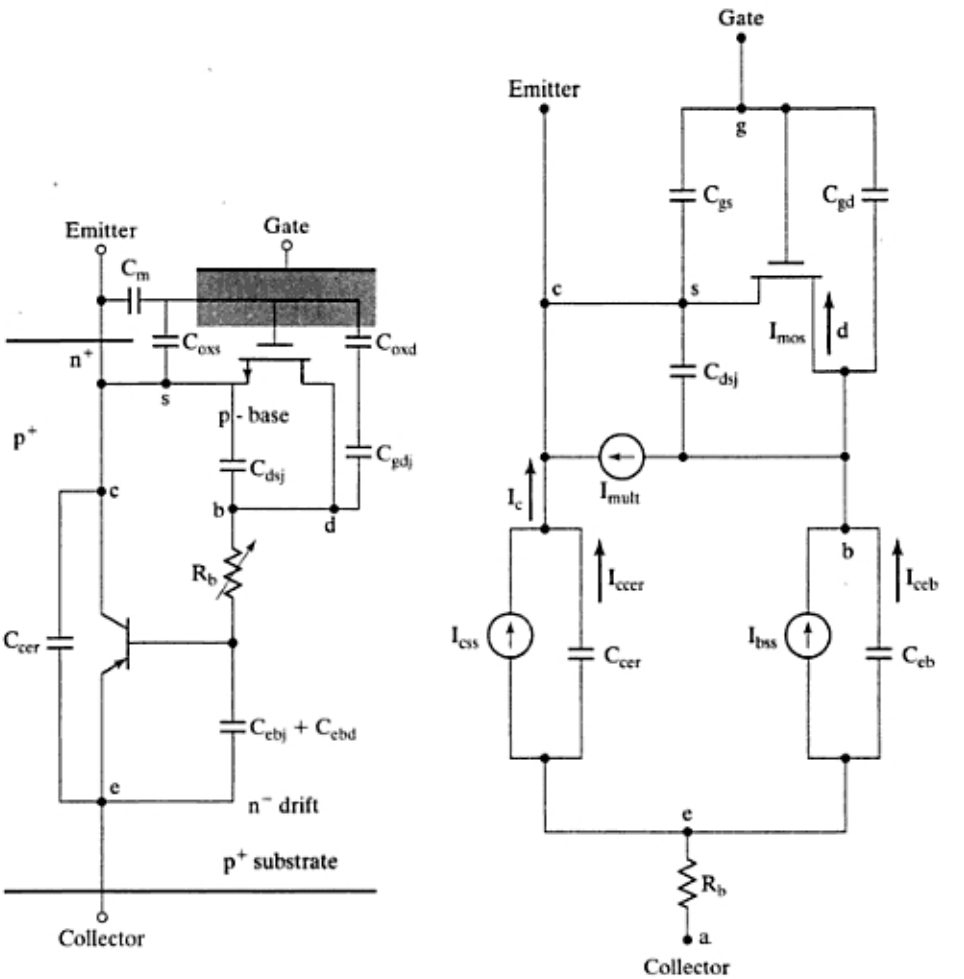
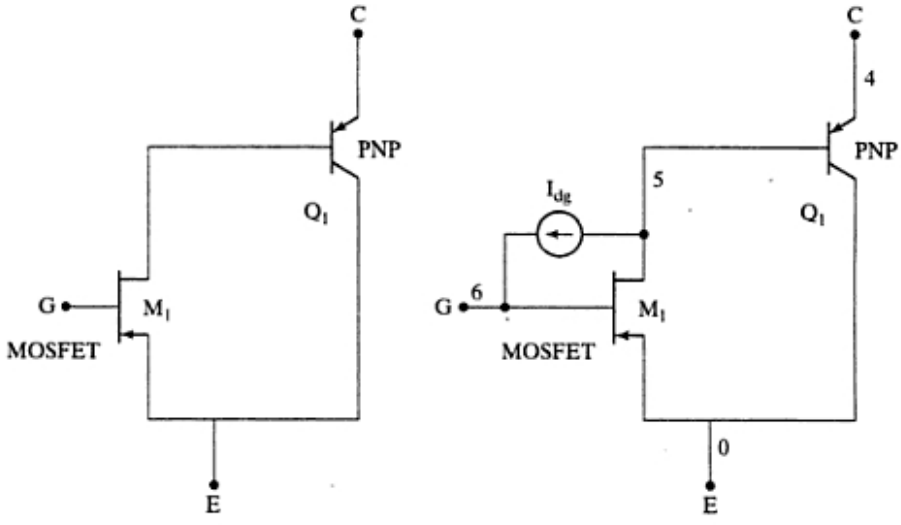


FIGURE 4.40
IGBT model. [Ref. 16, K. Shenai]

magnitude due to any changes in drain-to-gate voltage V_{dg}. This is, C_{dg} is expressed by

$$C_{dg} = \frac{\epsilon_{si} C_{oxd}}{\sqrt{\frac{2\epsilon_{si} V_{dg}}{qN_B}}\, C_{oxd} + A_{dg}\epsilon_{si}}$$

where A_{dg} is the area of the gate over the base;
ϵ_{si} is the dielectric constant of silicon;
C_{oxd} is the gate–drain overlap oxide capacitance;
q is the electron charge;
N_B is the base doping density.



(a) Composite model (b) Sheng PSpice model

FIGURE 4.41
Equivalent circuits of IGBT SPICE models. [Ref. 21, K. Sheng]

PSpice does not incorporate a capacitance model involving the square root, which models the space charge layer variation for a step junction. PSpice model can implement the equations describing the highly nonlinear gate–drain capacitance into the composite model by using the analog behavioral modeling function of PSpice.

4.10 COMPARISONS OF TRANSISTORS

Table 4.1 shows the comparisons of BJTs, MOSFETs, and IGBTs.

SUMMARY

Power transistors are generally of five types: BJTs, MOSFETs, SITs, IGBTs, and COOLMOS. BJTs are current-controlled devices and their parameters are sensitive to junction temperature. BJTs suffer from second breakdown and require reverse base current during turn-off to reduce the storage time, but they have low on-state or saturation voltage.

MOSFETs are voltage-controlled devices and require very low gating power and their parameters are less sensitive to junction temperature. There is no second breakdown problem and no need for negative gate voltage during turn-off. The conduction losses of COOLMOS devices is reduced by a factor of five as compared with those of the conventional technology. It is capable to handle two to three times more output power as compared with that of a standard MOSFET of the same package. IGBTs, which combine the advantages of BJTs and MOSFETs, are voltage-controlled devices and have low on-state voltage similar to BJTs. COOLMOS, which has very low on-state loss, is used in high-efficiency, low-power applications. IGBTs have no second

TABLE 4.1 Comparisons of Power Transistors

Switch Type	Base/Gate Control Variable	Control Characteristic	Switching Frequency	On-State Voltage Drop	Max. Voltage Rating V_s	Max. Current Rating I_s	Advantages	Limitations
BJT	Current	Continuous	Medium 20 kHz	Low	1.5 kV $S_s = V_s I_s$ = 1.5 MVA	1 kA $S_s = V_s I_s$ = 1.5 MVA	Simple switch Low on-state drop Higher off-state voltage capability High switching loss	Current controlled device and requires a higher base current to turn-on and sustain on-state current Base drive power loss Charge recovery time and slower switching speed Secondary breakdown region High switching losses Unipolar voltage device
MOSFET	Voltage	Continuous	Very high	High	1 kV $S_s = V_s I_s$ = 0.1 MVA	150 A $S_s = V_s I_s$ = 0.1 MVA	Higher switching speed Low switching loss Simple gate drive circuit Little gate power. Negative temperature coefficient on rain current and facilitates parallel operation	High on-state drop as high as 10 V Lower off-state voltage capability Unipolar voltage device
COOLMOS	Voltage	Continuous	Very high	Low	1 kV	100 A	Low gate drive requirement and low on-state power drop	Low-power device Low voltage and current ratings
IGBT	Voltage	Continuous	High	Medium	3.5 kV $S_s = V_s I_s$ = 1.5 MVA	2 kA $S_s = V_s I_s$ = 1.5 MVA	Low on-state voltage Little gate power	Lower off-state voltage capability Unipolar voltage device
SIT	Voltage	Continuous	Very high	High			High-voltage rating	Higher on-state voltage drop Lower current ratings

breakdown phenomena. SITs are high-power, high-frequency devices. They are most suitable for audio, VHF/UHF, and microwave amplifiers. They have a normally on-characteristic and a high on-state drop.

Transistors can be connected in series or parallel. Parallel operation usually requires current-sharing elements. Series operation requires matching of parameters, especially during turn-on and turn-off. To maintain the voltage and current relationship of transistors during turn-on and turn-off, it is generally necessary to use snubber circuits to limit the di/dt and dv/dt.

The gate signals can be isolated from the power circuit by pulse transformers or optocouplers. The pulse transformers are simple, but the leakage inductance should be very small. The transformers may be saturated at a low frequency and a long pulse. Optocouplers require separate power supply.

REFERENCES

[1] B. J. Baliga, *Power Semiconductor Devices*. Boston, MA: PWS Publishing. 1996.

[2] S. K. Ghandi, *Semiconductor Power Devices*. New York: John Wiley & Sons. 1977.

[3] S. M. Sze, *Modern Semiconductor Device Physics*. New York: John Wiley & Sons. 1998.

[4] B. I. Baliga and D. Y. Chen, *Power Transistors: Device Design and Applications*. New York: IEEE Press. 1984.

[5] Westinghouse Electric, *Silicon Power Transistor Handbook*. Pittsburgh: Westinghouse Electric Corp. 1967.

[6] R. Severns and J. Armijos, *MOSPOWER Application Handbook*. Santa Clara, CA: Siliconix Corp. 1984.

[7] S. Clemente and B. R. Pelly, "Understanding power MOSFET switching performance," *Solid-State Electronics*, Vol. 12, No. 12, 1982, pp. 1133–1141.

[8] D. A. Grant and I. Gower, *Power MOSFETs: Theory and Applications*. New York: John Wiley & Sons. 1988.

[9] L. Lorenz, G. Deboy, A. Knapp, and M. Marz, "COOLMOS™—a new milestone in high voltage power MOS," *Proc. ISPSD 99*, Toronto, 1999, pp. 3–10.

[10] G. Deboy, M. Marz, J. P. Stengl, H. Strack, J. Tilhanyi, and H. Weber, "A new generation of high voltage MOSFETs breaks the limit of silicon," *Proc. IEDM 98*, San Francisco, 1998, pp. 683–685.

[11] Infineon Technologies, *CoolMOS™: Power Semiconductors*. Germany: Siemens. 2001. www.infineon.co

[12] C. Hu, "Optimum doping profile for minimum ohmic resistance and high breakdown voltage," *IEEE Transactions on Electronic Devices*, Vol. ED-26, No. 3, 1979.

[13] B. J. Baliga, M. Cheng, P. Shafer, and M. W. Smith, "The insulated gate transistor (IGT): a new power switching device," IEEE Industry Applications Society Conference Record, 1983, pp. 354–363.

[14] B. J. Baliga, M. S. Adler, R. P. Love, P. V. Gray, and N. Zommer, "The insulated gate transistor: a new three-terminal MOS controlled bipolar power device," *IEEE Transactions Electron Devices*, ED-31, 1984, pp. 821–828.

[15] *IGBT Designer's Manual*. El Segundo, CA. International Rectifier, 1991.

[16] K. Shenai, *Power Electronics Handbook*, edited by M. H. Rashid. Los Angeles, CA: Academic Press. 2001, Chapter 7.

[17] I. Nishizawa and K. Yamamoto, "High-frequency high-power static induction transistor," *IEEE Transactions on Electron Devices*, Vol. ED25, No. 3, 1978, pp. 314–322.

[18] J. Nishizawa, T. Terasaki, and J. Shibata, "Field-effect transistor versus analog transistor (static induction transistor)," *IEEE Transactions on Electron Devices*, Vol. 22, No. 4, April 1975, pp. 185–197.

[19] B. M. Wilamowski, *Power Electronics Handbook*, edited by M. H. Rashid. Los Angeles, CA: Academic Press. 2001, Chapter 9.

[20] M. H. Rashid, *SPICE for Power Electronics and Electric Power*. Englewood Cliffs, NJ: Prentice-Hall. 1993.

[21] K. Sheng, S. J. Finney, and B. W. Williams, "Fast and accurate IGBT model for PSpice," *Electronics Letters*, Vol. 32, No. 25, December 5, 1996, pp. 2294–2295.

[22] A. G. M. Strollo, "A new IGBT circuit model for SPICE simulation," *Power Electronics Specialists Conference*, June 1997, Vol. 1, pp. 133–138.

[23] K. Sheng, S. J. Finney, and B. W. Williams, "A new analytical IGBT model with improved electrical characteristics," *IEEE Transactions on Power Electronics*, Vol. 14, No. 1, January 1999, pp. 98–107.

[24] K. Sheng, B. W. Williams, and S. J. Finney, "A review of IGBT models," *IEEE Transactions on Power Electronics*, Vol. 15, No. 6, November 2000, pp. 1250–1266.

[25] A. R. Hefner, "An investigation of the drive circuit requirements for the power insulated gate bipolar transistor (IGBT)," *IEEE Transactions on Power Electronics*, Vol. 6, 1991, pp. 208–219.

[26] C. Licitra, S. Musumeci, A. Raciti, A. U. Galluzzo, and R. Letor, "A new driving circuit for IGBT devices," *IEEE Transactions Power Electronics*, Vol. 10, 1995, pp. 373–378.

[27] H. G. Lee, Y. H. Lee, B. S. Suh, and J. W. Lee, "A new intelligent gate control scheme to drive and protect high power IGBTs," *European Power Electronics Conference Records*, 1997, pp. 1.400–1.405.

[28] S. Bernet, "Recent developments of high power converters for industry and traction applications," *IEEE Transactions on Power Electronics*, Vol. 15, No. 6, November 2000, pp. 1102–1117.

REVIEW QUESTIONS

4.1 What is a bipolar transistor (BJT)?
4.2 What are the types of BJTs?
4.3 What are the differences between *NPN*-transistors and *PNP*-transistors?
4.4 What are the input characteristics of *NPN*-transistors?
4.5 What are the output characteristics of *NPN*-transistors?
4.6 What are the three regions of operation for BJTs?
4.7 What is a beta (β) of BJTs?
4.8 What is the difference between beta, β, and forced beta, β_F of BJTs?
4.9 What is a transductance of BJTs?
4.10 What is an overdrive factor of BJTs?
4.11 What is the switching model of BJTs?
4.12 What is the cause of delay time in BJTs?
4.13 What is the cause of storage time in BJTs?
4.14 What is the cause of rise time in BJTs?
4.15 What is the cause of fall time in BJTs?
4.16 What is a saturation mode of BJTs?

4.17 What is a turn-on time of BJTs?
4.18 What is a turn-off time of BJTs?
4.19 What is a FBSOA of BJTs?
4.20 What is a RBSOA of BJTs?
4.21 Why is it necessary to reverse bias BJTs during turn-off?
4.22 What is a second breakdown of BJTs?
4.23 What are the advantages and disadvantages of BJTs?
4.24 What is an MOSFET?
4.25 What are the types of MOSFETs?
4.26 What are the differences between enhancement-type MOSFETs and depletion-type MOSFETs?
4.27 What is a pinch-off voltage of MOSFETs?
4.28 What is a threshold voltage of MOSFETs?
4.29 What is a transconductance of MOSFETs?
4.30 What is the switching model of *n*-channel MOSFETs?
4.31 What are the transfer characteristics of MOSFETs?
4.32 What are the output characteristics of MOSFETs?
4.33 What are the advantages and disadvantages of MOSFETs?
4.34 Why do the MOSFETs not require negative gate voltage during turn-off?
4.35 Why does the concept of saturation differ in BJTs and MOSFETs?
4.36 What is a turn-on time of MOSFETs?
4.37 What is a turn-off time of MOSFETs?
4.38 What is an SIT?
4.39 What are the advantages of SITs?
4.40 What are the disadvantages of SITs?
4.41 What is an IGBT?
4.42 What are the transfer characteristics of IGBTs?
4.43 What are the output characteristics of IGBTs?
4.44 What are the advantages and disadvantages of IGBTs?
4.45 What are the main differences between MOSFETs and BJTs?
4.46 What are the problems of parallel operation of BJTs?
4.47 What are the problems of parallel operation of MOSFETs?
4.48 What are the problems of parallel operation of IGBTs?
4.49 What are the problems of series operation of BJTs?
4.50 What are the problems of series operations of MOSFETs?
4.51 What are the problems of series operations of IGBTs?
4.52 What are the purposes of shunt snubber in transistors?
4.53 What is the purpose of series snubber in transistors?

PROBLEMS

4.1 The beta (β) of bipolar transistor in Figure 4.7 varies from 10 to 60. The load resistance is $R_C = 5\ \Omega$. The dc supply voltage is $V_{CC} = 100$ V and the input voltage to the base circuit is $V_B = 8$ V. If $V_{CE(sat)} = 2.5$ V and $V_{BE(sat)} = 1.75$ V, find **(a)** the value of R_B that will result in saturation with an overdrive factor of 20; **(b)** the forced β, and **(c)** the power loss in the transistor P_T.

4.2 The beta (β) of bipolar transistor in Figure 4.7 varies from 12 to 75. The load resistance is $R_C = 1.5\ \Omega$. The dc supply voltage is $V_{CC} = 40$ V and the input voltage to the base circuit is $V_B = 6$ V. If $V_{CE(sat)} = 1.2$ V, $V_{BE(sat)} = 1.6$ V, and $R_B = 0.7\ \Omega$, determine **(a)** the ODF, **(b)** the forced β, and **(c)** the power loss in the transistor P_T.

4.3 A transistor is used as a switch and the waveforms are shown in Figure 4.11. The parameters are $V_{CC} = 200$ V, $V_{BE(sat)} = 3$ V, $I_B = 8$ A, $V_{CE(sat)} = 2$ V, $I_{CS} = 100$ A, $t_d = 0.5$ μs, $t_r = 1$ μs, $t_s = 5$ μs, $t_f = 3$ μs, and $f_s = 10$ kHz. The duty cycle is $k = 50\%$. The collector–emitter leakage current is $I_{CEO} = 3$ mA. Determine the power loss due to the collector current **(a)** during turn-on $t_{on} = t_d + t_r$; **(b)** during conduction period t_n, **(c)** during turn-off $t_{off} = t_s + t_f$, **(d)** during off-time t_o, and **(e)** the total average power losses P_T. **(f)** Plot the instantaneous power due to the collector current $P_c(t)$.

4.4 The maximum junction temperature of the bipolar transistor in Problem 4.3 is $T_j = 150°C$ and the ambient temperature is $T_A = 25°C$. If the thermal resistances are $R_{JC} = 0.4°C/W$ and $R_{CS} = 0.05°C/W$, calculate the thermal resistance of heat sink R_{SA}. (*Hint*: Neglect the power loss due to base drive.)

4.5 For the parameters in Problem 4.3, calculate the average power loss due to the base current P_B.

4.6 Repeat Problem 4.3 if $V_{BE(sat)} = 2.3$ V, $I_B = 8$ A, $V_{CE(sat)} = 1.4$ V, $t_d = 0.1$ μs, $t_r = 0.45$ μs, $t_s = 3.2$ μs, and $t_f = 1.1$ μs.

4.7 An MOSFET is used as a switch. The parameters are $V_{DD} = 40$ V, $I_D = 35$ A, $R_{DS} = 28$ mΩ, $V_{GS} = 10$ V, $t_{d(on)} = 25$ ns, $t_r = 60$ ns, $t_{d(off)} = 70$ ns, $t_f = 25$ ns, and $f_s = 20$ kHz. The drain source leakage current is $I_{DSS} = 250$ μA. The duty cycle is $k = 60\%$. Determine the power loss due to the drain current **(a)** during turn-on $t_{on} = t_{d(n)} + t_r$; **(b)** during conduction period t_n, **(c)** during turn-off $t_{off} = t_{d(off)} + t_f$, **(d)** during off-time t_o, and **(e)** the total average power losses P_T.

4.8 The maximum junction temperature of the MOSFET in Problem 4.7 is $T_j = 150°C$ and the ambient temperature is $T_A = 30°C$. If the thermal resistances are $R_{JC} = 1$ K/W and $R_{CS} = 1$ K/W, calculate the thermal resistance of the heat sink R_{SA}. (*Note*: $K = °C + 273$.)

4.9 Two BJTs are connected in parallel similar to Figure 4.32. The total load current of $I_T = 200$ A. The collector–emitter voltage of transistor Q_1 is $V_{CE1} = 1.5$ V and that of transistor Q_2 is $V_{CE2} = 1.1$ V. Determine the collector current of each transistor and difference in current sharing if the current sharing series resistances are **(a)** $R_{e1} = 10$ mΩ and $R_{e2} = 20$ mΩ, and **(b)** $R_{e1} = R_{e2} = 20$ mΩ.

4.10 A bipolar transistor is operated as a chopper switch at a frequency of $f_s = 20$ kHz. The circuit arrangement is shown in Figure 4.35a. The dc input voltage of the chopper is $V_s = 400$ V and the load current is $I_L = 100$ A. The switching times are $t_r = 1$ μs and $t_f = 3$ μs. Determine the values of **(a)** L_s; **(b)** C_s; **(c)** R_s for critically damped condition; **(d)** R_s if the discharge time is limited to one-third of switching period; **(e)** R_s if peak discharge current is limited to 5% of load current; and **(f)** power loss due to RC snubber P_s, neglecting the effect of inductor L_s on the voltage of snubber capacitor C_s. Assume that $V_{CE(sat)} = 0$.

4.11 An MOSFET is operated as a chopper switch at a frequency of $f_s = 50$ kHz. The circuit arrangement is shown in Figure 4.35a. The dc input voltage of the chopper is $V_s = 30$ V and the load current is $I_L = 40$ A. The switching times are $t_r = 60$ ns and $t_f = 25$ ns. Determine the values of **(a)** L_s; **(b)** C_s; **(c)** R_s for critically damped condition; **(d)** R_s if the discharge time is limited to one-third of switching period; **(e)** R_s if peak discharge current is limited to 5% of load current; and **(f)** power loss due to RC snubber P_s, neglecting the effect of inductor L_s on the voltage of snubber capacitor C_s. Assume that $V_{CE(sat)} = 0$.

CHAPTER 5

Dc–Dc Converters

The learning objectives of this chapter are as follows:

- To learn the switching technique for dc–dc conversion and the types of dc–dc converters
- To study the operation of dc–dc converters
- To understand the performance parameters of dc converters
- To learn the techniques for the analysis and design of dc converters
- To learn the techniques for simulating dc converters by using SPICE
- To study effects of load inductance on the load current and the conditions for continuous current

5.1 INTRODUCTION

In many industrial applications, it is required to convert a fixed-voltage dc source into a variable-voltage dc source. A dc–dc converter converts directly from dc to dc and is simply known as a dc converter. A dc converter can be considered as dc equivalent to an ac transformer with a continuously variable turns ratio. Like a transformer, it can be used to step down or step up a dc voltage source.

Dc converters are widely used for traction motor control in electric automobiles, trolley cars, marine hoists, forklift trucks, and mine haulers. They provide smooth acceleration control, high efficiency, and fast dynamic response. Dc converters can be used in regenerative braking of dc motors to return energy back into the supply, and this feature results in energy savings for transportation systems with frequent stops. Dc converters are used in dc voltage regulators; and also are used, in conjunction with an inductor, to generate a dc current source, especially for the current source inverter.

5.2 PRINCIPLE OF STEP-DOWN OPERATION

The principle of operation can be explained by Figure 5.1a. When switch SW, known as the chopper, is closed for a time t_1, the input voltage V_s appears across the load. If the switch remains off for a time t_2, the voltage across the load is zero. The waveforms for the output voltage and load current are also shown in Figure 5.1b. The converter switch can be implemented by using a (1) power bipolar junction transistor (BJT), (2) power metal oxide semiconductor field-effect transistor (MOSFET), (3) gate-turn-off thyristor (GTO), or (4) insulated-gate bipolar transistor (IGBT). The

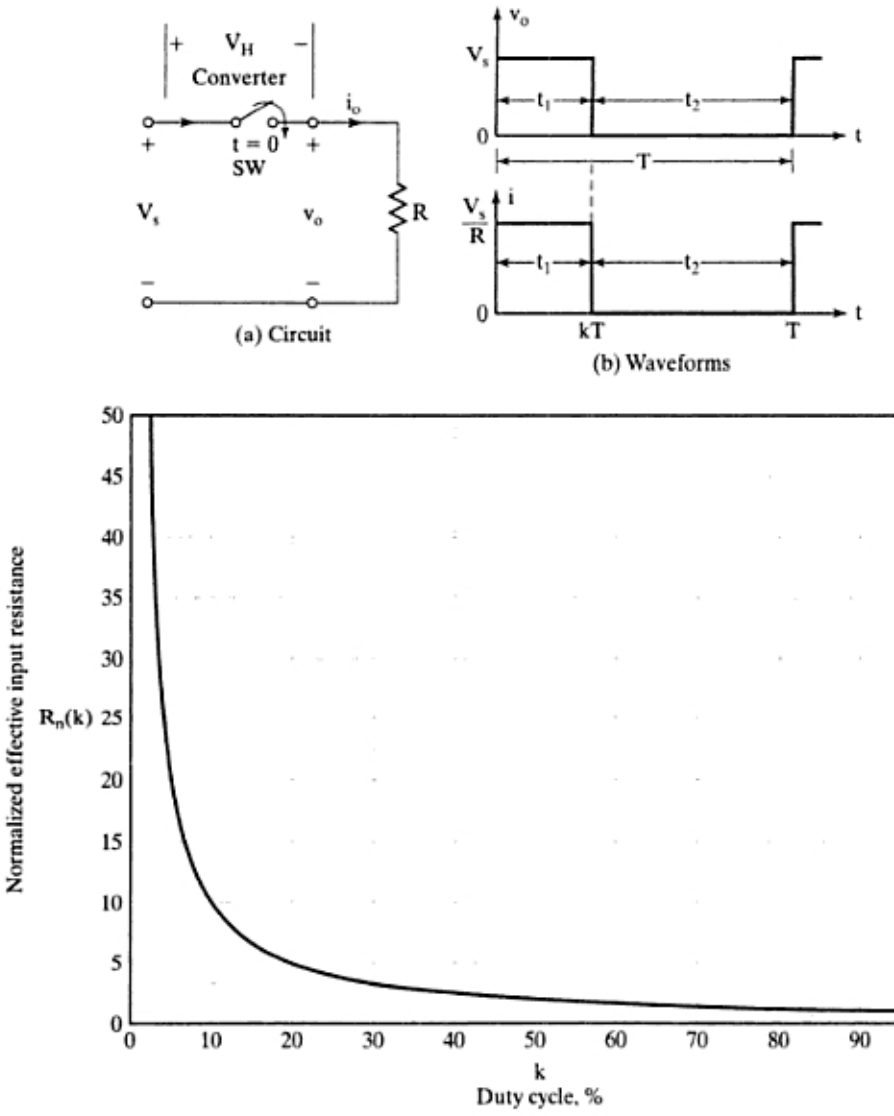


FIGURE 5.1

Step-down converter with resistive load.

practical devices have a finite voltage drop ranging from 0.5 to 2 V, and for the sake of simplicity we shall neglect the voltage drops of these power semiconductor devices.

The average output voltage is given by

$$V_a = \frac{1}{T}\int_0^{t_1} v_0\, dt = \frac{t_1}{T} V_s = f t_1 V_s = k V_s \tag{5.1}$$

and the average load current, $I_a = V_a/R = kV_s/R$,

where T is the chopping period;
$k = t_1/T$ is the duty cycle of chopper;
f is the chopping frequency.

The rms value of output voltage is found from

$$V_o = \left(\frac{1}{T}\int_0^{kT} v_0^2\, dt\right)^{1/2} = \sqrt{k}\, V_s \tag{5.2}$$

Assuming a lossless converter, the input power to the converter is the same as the output power and is given by

$$P_i = \frac{1}{T}\int_0^{kT} v_0 i\, dt = \frac{1}{T}\int_0^{kT} \frac{v_0^2}{R}\, dt = k\frac{V_s^2}{R} \tag{5.3}$$

The effective input resistance seen by the source is

$$R_i = \frac{V_s}{I_a} = \frac{V_s}{kV_s/R} = \frac{R}{k} \tag{5.4}$$

which indicates that the converter makes the input resistance R_i as a variable resistance of R/k. The variation of the normalized input resistance against the duty cycle is shown in Figure 5.1c. It should be noted that the switch in Figure 5.1 could be implemented by a BJT, an MOSFET, an IGBT, or a GTO.

The duty cycle k can be varied from 0 to 1 by varying t_1, T, or f. Therefore, the output voltage V_o can be varied from 0 to V_s by controlling k, and the power flow can be controlled.

1. *Constant-frequency operation*: The converter, or switching, frequency f (or chopping period T) is kept constant and the on-time t_1 is varied. The width of the pulse is varied and this type of control is known as *pulse-width-modulation* (PWM) control.
2. *Variable-frequency operation*: The chopping, or switching, frequency f is varied. Either on-time t_1 or off-time t_2 is kept constant. This is called *frequency modulation*. The frequency has to be varied over a wide range to obtain the full output voltage range. This type of control would generate harmonics at unpredictable frequencies and the filter design would be difficult.

Example 5.1 Finding the Performances of a Dc–Dc Converter

The dc converter in Figure 5.1a has a resistive load of $R = 10\ \Omega$ and the input voltage is $V_s = 220$ V. When the converter switch remains on, its voltage drop is $v_{ch} = 2$ V and the chopping frequency is $f = 1$ kHz. If the duty cycle is 50%, determine (a) the average output voltage V_a, (b) the rms output voltage V_o, (c) the converter efficiency, (d) the effective input resistance R_i of the converter, and (e) the rms value of the fundamental component of output harmonic voltage.

Solution

$V_s = 220$ V, $k = 0.5$, $R = 10\ \Omega$, and $v_{ch} = 2$ V.

a. From Eq. (5.1), $V_a = 0.5 \times (220 - 2) = 109$ V.
b. From Eq. (5.2), $V_o = \sqrt{0.5} \times (220 - 2) = 154.15$ V.

c. The output power can be found from

$$P_o = \frac{1}{T}\int_0^{kT} \frac{v_0^2}{R}\,dt = \frac{1}{T}\int_0^{kT} \frac{(V_s - v_{ch})^2}{R}\,dt = k\frac{(V_s - v_{ch})^2}{R}$$
$$= 0.5 \times \frac{(220 - 2)^2}{10} = 2376.2\ \text{W} \tag{5.5}$$

The input power to the converter can be found from

$$P_i = \frac{1}{T}\int_0^{kT} V_s i\,dt = \frac{1}{T}\int_0^{kT} \frac{V_s(V_s - v_{ch})}{R}\,dt = k\frac{V_s(V_s - v_{ch})}{R}$$
$$= 0.5 \times 220 \times \frac{220 - 2}{10} = 2398\ \text{W} \tag{5.6}$$

The converter efficiency is

$$\frac{P_o}{P_i} = \frac{2376.2}{2398} = 99.09\%$$

d. From Eq. (5.4), $R_i = 10/0.5 = 20\ \Omega$.

e. The output voltage as shown in Figure 5.1b can be expressed in a Fourier series as

$$v_o(t) = kV_s + \frac{V_s}{n\pi}\sum_{n=1}^{\infty} \sin 2n\pi k \cos 2n\pi ft$$
$$+ \frac{V_s}{n\pi}\sum_{n=1}^{\infty}(1 - \cos 2n\pi k)\sin 2n\pi ft \tag{5.7}$$

The fundamental component (for $n = 1$) of output voltage harmonic can be determined from Eq. (5.7) as

$$v_1(t) = \frac{V_s}{\pi}[\sin 2\pi k \cos 2\pi ft + (1 - \cos 2\pi k)\sin 2\pi ft]$$
$$= \frac{220 \times 2}{\pi}\sin(2\pi \times 1000t) = 140.06\sin(6283.2t) \tag{5.8}$$

and its root-mean-square (rms) value is $V_1 = 140.06/\sqrt{2} = 99.04$ V.

Note: The efficiency calculation, which includes the conduction loss of the converter, does not take into account the switching loss due to turn-on and turn-off of practical converters. The efficiency of a practical converter varies between 92 and 99%.

Key Points of Section 5.2

- A step-down chopper, or dc converter, that acts as a variable resistance load can produce an output voltage from 0 to V_S.

- Although a dc converter can be operated either at a fixed or variable frequency, it is usually operated at a fixed frequency with a variable duty cycle.
- The output voltage contains harmonics and a dc filter is needed to smooth out the ripples.

5.2.1 Generation of Duty Cycle

The duty cycle k can be generated by comparing a dc reference signal v_r with a saw-tooth carrier signal v_{cr}. This is shown in Figure 5.2, where V_r is the peak value of v_r, and V_{cr} is the peak value of v_{cr}. The reference signal v_r is given by

$$v_r = \frac{V_r}{T}t \tag{5.9}$$

which must equal to the carrier signal $v_{cr} = V_{cr} = kT$. That is,

$$V_{cr} = \frac{V_r}{T}kT$$

which gives the duty cycle duty k as

$$k = \frac{V_{cr}}{V_r} = M \tag{5.10}$$

where M is called the *modulation index*. By varying the carrier signal v_{cr} from 0 to V_{cr}, the duty cycle k can be varied from 0 to 1.

The algorithm to generate the gating signal is as follows:

1. Generate a triangular waveform of period T as the reference signal v_r and a dc carrier signal v_{cr}.
2. Compare these signals by a comparator to generate the difference $v_c - v_{cr}$ and then a hard limiter to obtain a square-wave gate pulse of width kT, which must be applied to the switching device through an isolating circuit.
3. Any variation in v_{cr} varies linearly with the duty cycle k.

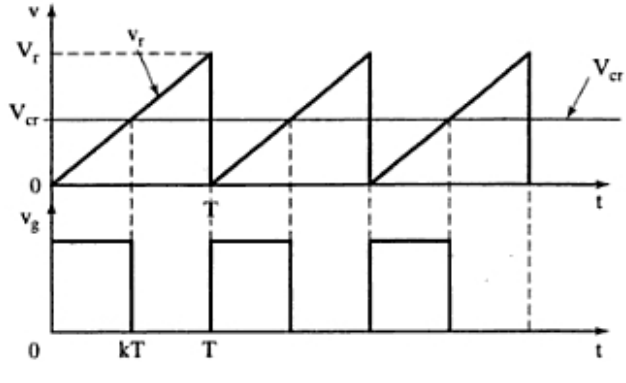


FIGURE 5.2

Comparing a reference signal with a carrier signal.

5.3 STEP-DOWN CONVERTER WITH *RL* LOAD

A converter [1] with an RL load is shown in Figure 5.3. The operation of the converter can be divided into two modes. During mode 1, the converter is switched on and the current flows from the supply to the load. During mode 2, the converter is switched off and the load current continues to flow through freewheeling diode D_m. The equivalent circuits for these modes are shown in Figure 5.4a. The load current and output voltage waveforms are shown in Figure 5.4b with the assumption that the load current rises linearly. However, the current flowing through an RL load rises or falls exponentially with a time constant. The load time constant ($\tau = L/R$) is generally much higher than the switching period T. Thus, the linear approximation is valid for many circuit conditions and simplified expressions can be derived within reasonable accuracies.

The load current for mode 1 can be found from

$$V_s = Ri_1 + L\frac{di_1}{dt} + E$$

which with initial current $i_1(t = 0) = I_1$ gives the load current as

$$i_1(t) = I_1 e^{-tR/L} + \frac{V_s - E}{R}(1 - e^{-tR/L}) \tag{5.11}$$

This mode is valid $0 \le t \le t_1 (= kT)$; and at the end of this mode, the load current becomes

$$i_1(t = t_1 = kT) = I_2 \tag{5.12}$$

The load current for mode 2 can be found from

$$0 = Ri_2 + L\frac{di_2}{dt} + E$$

With initial current $i_2(t = 0) = I_2$ and redefining the time origin (i.e., $t = 0$) at the beginning of mode 2, we have

$$i_2(t) = I_2 e^{-tR/L} - \frac{E}{R}(1 - e^{-tR/L}) \tag{5.13}$$

This mode is valid for $0 \le t \le t_2 [= (1 - k)T]$. At the end of this mode, the load current becomes

$$i_2(t = t_2) = I_3 \tag{5.14}$$

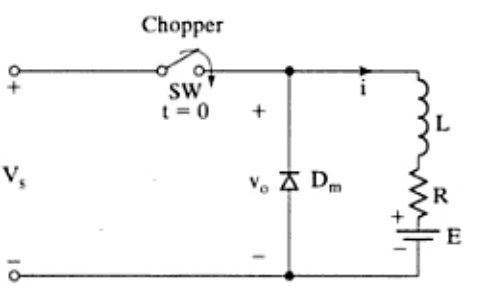


FIGURE 5.3
Dc converter with RL loads.

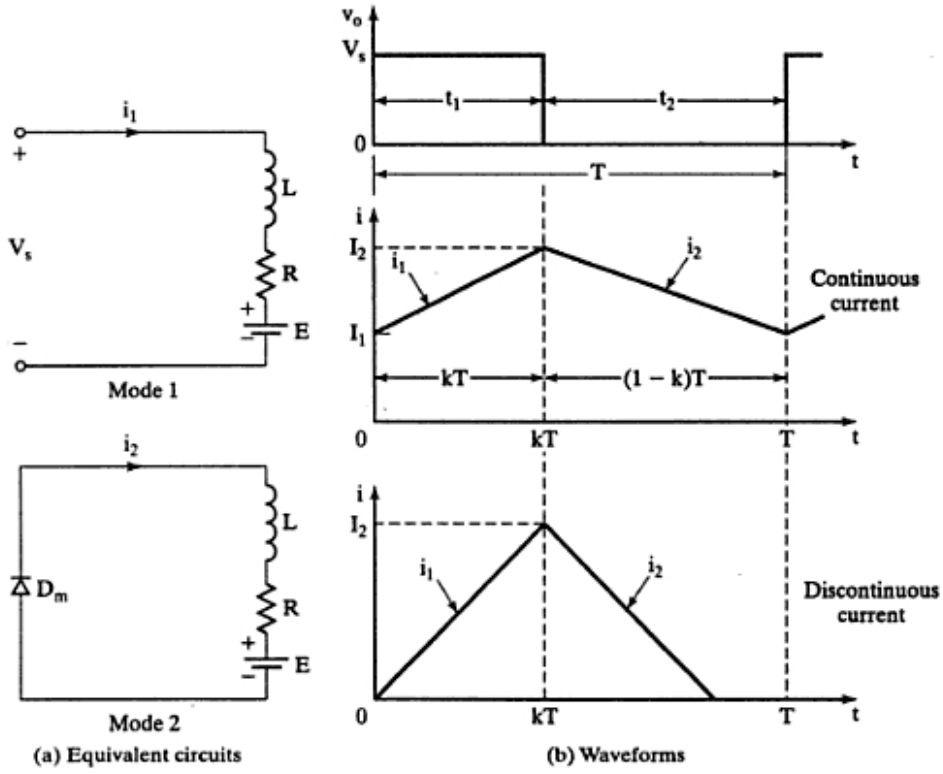


FIGURE 5.4

Equivalent circuits and waveforms for *RL* loads.

At the end of mode 2, the converter is turned on again in the next cycle after time, $T = 1/f = t_1 + t_2$.

Under steady-state conditions, $I_1 = I_3$. The peak-to-peak load ripple current can be determined from Eqs. (5.11) to (5.14). From Eqs. (5.11) and (5.12), I_2 is given by

$$I_2 = I_1 e^{-kTR/L} + \frac{V_s - E}{R}(1 - e^{-kTR/L}) \tag{5.15}$$

From Eqs. (5.13) and (5.14), I_3 is given by

$$I_3 = I_1 = I_2 e^{-(1-k)TR/L} - \frac{E}{R}(1 - e^{-(1-k)TR/L}) \tag{5.16}$$

Solving for I_1 and I_2, we get

$$I_1 = \frac{V_S}{R}\left(\frac{e^{kz} - 1}{e^z - 1}\right) - \frac{E}{R} \tag{5.17}$$

where $z = \dfrac{TR}{L}$ is the ratio of the chopping or switching period to the load time constant.

$$I_2 = \frac{V_s}{R}\left(\frac{e^{-kz} - 1}{e^{-z} - 1}\right) - \frac{E}{R} \tag{5.18}$$

The peak-to-peak ripple current is

$$\Delta I = I_2 - I_1$$

which after simplifications becomes

$$\Delta I = \frac{V_s}{R}\frac{1 - e^{-kz} + e^{-z} - e^{-(1-k)z}}{1 - e^{-z}} \tag{5.19}$$

The condition for maximum ripple,

$$\frac{d(\Delta I)}{dk} = 0 \tag{5.20}$$

gives $e^{-kz} - e^{-(1-k)z} = 0$ or $-k = -(1 - k)$ or $k = 0.5$. The maximum peak-to-peak ripple current (at $k = 0.5$) is

$$\Delta I_{\max} = \frac{V_s}{R}\tanh\frac{R}{4fL} \tag{5.21}$$

For $4fL >> R$, $\tanh\theta \approx \theta$ and the maximum ripple current can be approximated to

$$\Delta I_{\max} = \frac{V_s}{4fL} \tag{5.22}$$

Note: Equations (5.11) to (5.22) are valid only for continuous current flow. For a large off-time, particularly at low-frequency and low-output voltage, the load current may be discontinuous. The load current would be continuous if $L/R >> T$ or $Lf >> R$. In case of discontinuous load current, $I_1 = 0$ and Eq. (5.11) becomes

$$i_1(t) = \frac{V_s - E}{R}(1 - e^{-tR/L})$$

and Eq. (5.13) is valid for $0 \le t \le t_2$ such that $i_2(t = t_2) = I_3 = I_1 = 0$, which gives

$$t_2 = \frac{L}{R}\ln\left(1 + \frac{RI_2}{E}\right)$$

Because $t = kT$, we get

$$i_1(t) = I_2 = \frac{V_s - E}{R}\left(1 - e^{-kz}\right)$$

which after substituting for I_2 becomes

$$t_2 = \frac{L}{R}\ln\left[1 + \left(\frac{V_s - E}{E}\right)\left(1 - e^{-z}\right)\right]$$

Condition for continuous current: For $I_1 \geq 0$, Eq. (5.17) gives

$$\left(\frac{e^{kz}-1}{e^{z}-1} - \frac{E}{V_s}\right) \geq 0$$

which gives the value of the load electromotive force (emf) ratio $x = E/V_s$ as

$$x = \frac{E}{V_s} \leq \frac{e^{kz}-1}{e^{z}-1} \tag{5.23}$$

Example 5.2 Finding the Currents of a Dc Converter with an *RL* Load

A converter is feeding an *RL* load as shown in Figure 5.3 with $V_s = 220$ V, $R = 5\ \Omega$, $L = 7.5$ mH, $f = 1$ kHz, $k = 0.5$, and $E = 0$ V. Calculate (a) the minimum instantaneous load current I_1, (b) the peak instantaneous load current I_2, (c) the maximum peak-to-peak load ripple current, (d) the average value of load current I_a, (e) the rms load current I_o, (f) the effective input resistance R_i seen by the source, (g) the rms chopper current I_R, and (h) the critical value of the load inductance for continuous load current. Use PSpice to plot the load current, the supply current, and the freewheeling diode current.

Solution

$V_s = 220$ V, $R = 5\ \Omega$, $L = 7.5$ mH, $E = 0$ V, $k = 0.5$, and $f = 1000$ Hz. From Eq. (5.15), $I_2 = 0.7165I_1 + 12.473$ and from Eq. (5.16), $I_1 = 0.7165I_2 + 0$.

a. Solving these two equations yields $I_1 = 18.37$ A.

b. $I_2 = 25.63$ A.

c. $\Delta I = I_2 - I_1 = 25.63 - 18.37 = 7.26$ A. From Eq. (5.21), $\Delta I_{max} = 7.26$ A and Eq. (5.22) gives the approximate value, $\Delta I_{max} = 7.33$ A.

d. The average load current is, approximately,

$$I_a = \frac{I_2 + I_1}{2} = \frac{25.63 + 18.37}{2} = 22 \text{ A}$$

e. Assuming that the load current rises linearly from I_1 to I_2, the instantaneous load current can be expressed as

$$i_1 = I_1 + \frac{\Delta I t}{kT} \qquad \text{for } 0 < t < kT$$

The rms value of load current can be found from

$$I_o = \left(\frac{1}{kT}\int_0^{kT} i_1^2\, dt\right)^{1/2} = \left[I_1^2 + \frac{(I_2 - I_1)^2}{3} + I_1(I_2 - I_1)\right]^{1/2} \tag{5.24}$$

$$= 22.1 \text{ A}$$

f. The average source current

$$I_s = kI_a = 0.5 \times 22 = 11 \text{ A}$$

and the effective input resistance $R_i = V_s/I_s = 220/11 = 20\ \Omega$.

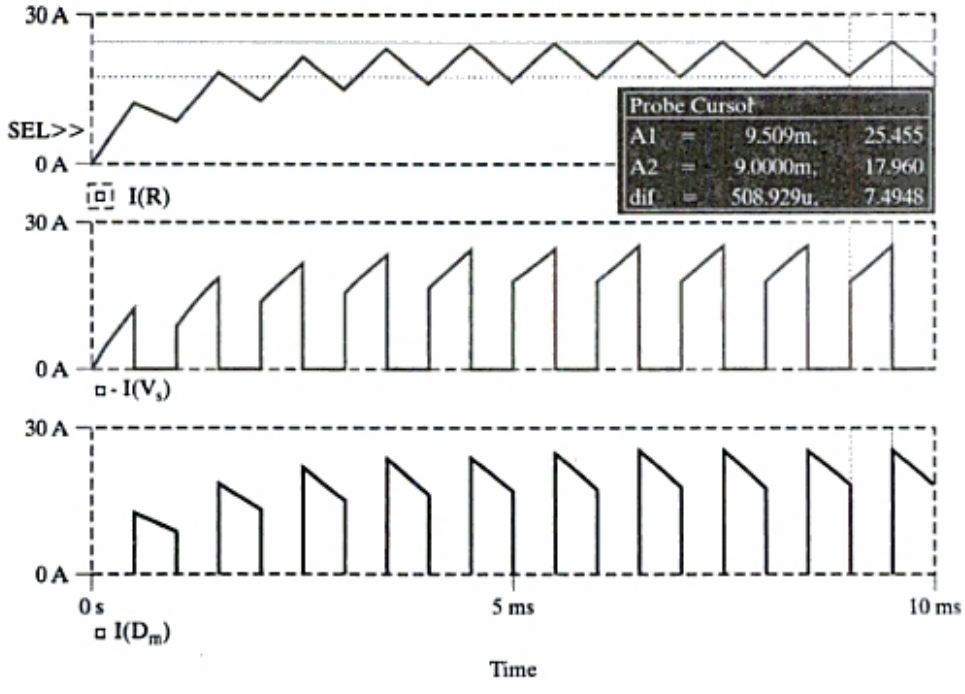


FIGURE 5.5

SPICE plots of load, input, and diode currents for Example 5.2.

g. The rms converter current can be found from

$$I_R = \left(\frac{1}{T}\int_0^{kT} i_1^2\,dt\right)^{1/2} = \sqrt{k}\left[I_1^2 + \frac{(I_2 - I_1)^2}{3} + I_1(I_2 - I_1)\right]^{1/2} \tag{5.25}$$

$$= \sqrt{k}I_o = \sqrt{0.5} \times 22.1 = 15.63\ \text{A}$$

h. We can rewrite Eq. (5.23) as

$$V_S\left(\frac{e^{kz} - 1}{e^z - 1}\right) = E$$

which, after iteration, gives, $z = TR/L = 52.5$ and $L = 1\ \text{ms} \times 5/52.5 = 0.096\ \text{mH}$. The SPICE simulation results [32] are shown in Figure 5.5, which shows the load current $I(E)$, the supply current $-I(V_s)$, and the diode current $I(D_m)$. We get $I_1 = 17.96$ A and $I_2 = 25.46$ A.

Example 5.3 Finding the Load Inductance to Limit the Load Ripple Current

The converter in Figure 5.3 has a load resistance $R = 0.25\ \Omega$, input voltage $V_s = 550$ V, and battery voltage $E = 0$ V. The average load current $I_a = 200$ A, and chopping frequency

$f = 250$ Hz. Use the average output voltage to calculate the load inductance L, which would limit the maximum load ripple current to 10% of I_a.

Solution

$V_s = 550$ V, $R = 0.25\ \Omega$, $E = 0$ V, $f = 250$ Hz, $T = 1/f = 0.004$ s, and $\Delta i = 200 \times 0.1 = 20$ A. The average output voltage $V_a = kV_s = RI_a$. The voltage across the inductor is given by

$$L\frac{di}{dt} = V_s - RI_a = V_s - kV_s = V_s(1 - k)$$

If the load current is assumed to rise linearly, $dt = t_1 = kT$ and $di = \Delta i$:

$$\Delta i = \frac{V_s(1 - k)}{L} kT$$

For the worst-case ripple conditions,

$$\frac{d(\Delta i)}{dk} = 0$$

This gives $k = 0.5$ and

$$\Delta i\, L = 20 \times L = 550(1 - 0.5) \times 0.5 \times 0.004$$

and the required value of inductance is $L = 27.5$ mH.

Note: For $\Delta I = 20$ A, Eq. (5.19) gives $z = 0.036$ and $L = 27.194$ mH.

Key Points of Section 5.3

- An inductive load can make the load current continuous. However, the critical value of inductance, which is required for continuous current, is influenced by the load emf ratio. The peak-to-peak load current ripple becomes maximum at $k = 0.5$.

5.4 PRINCIPLE OF STEP-UP OPERATION

A converter can be used to step up a dc voltage and an arrangement for step-up operation is shown in Figure 5.6a. When switch SW is closed for time t_1, the inductor current rises and energy is stored in the inductor L. If the switch is opened for time t_2, the energy stored in the inductor is transferred to load through diode D_1 and the inductor current falls. Assuming a continuous current flow, the waveform for the inductor current is shown in Figure 5.6b.

When the converter is turned on, the voltage across the inductor is

$$v_L = L\frac{di}{dt}$$

and this gives the peak-to-peak ripple current in the inductor as

$$\Delta I = \frac{V_s}{L} t_1 \tag{5.26}$$

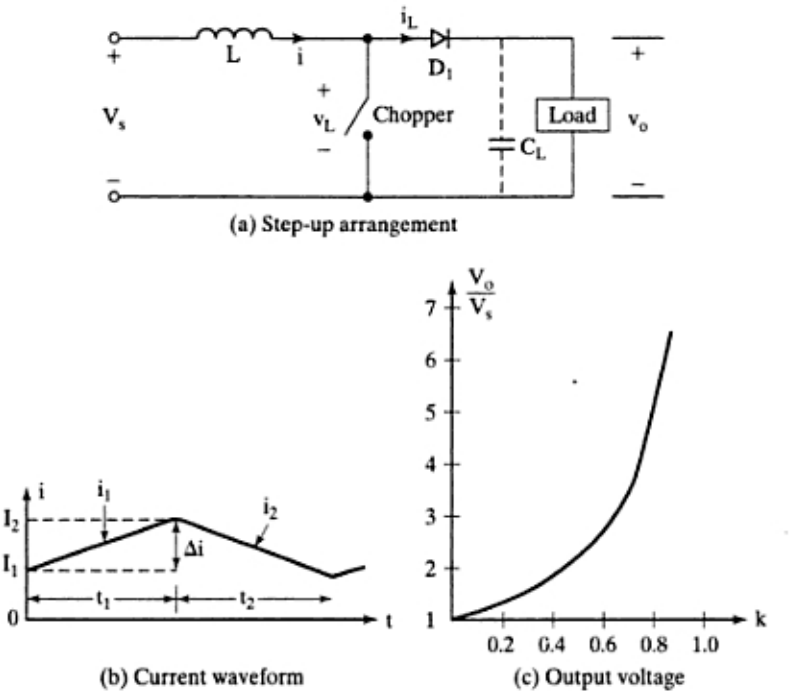


FIGURE 5.6

Arrangement for step-up operation.

The average output voltage is

$$v_o = V_s + L\frac{\Delta I}{t_2} = V_s\left(1 + \frac{t_1}{t_2}\right) = V_s\frac{1}{1-k} \tag{5.27}$$

If a large capacitor C_L is connected across the load as shown by dashed lines in Figure 5.6a, the output voltage is continuous and v_o becomes the average value V_a. We can notice from Eq. (5.27) that the voltage across the load can be stepped up by varying the duty cycle k and the minimum output voltage is V_s when $k = 0$. However, the converter cannot be switched on continuously such that $k = 1$. For values of k tending to unity, the output voltage becomes very large and is very sensitive to changes in k, as shown in Figure 5.6c.

This principle can be applied to transfer energy from one voltage source to another as shown in Figure 5.7a. The equivalent circuits for the modes of operation are shown in Figure 5.7b and the current waveforms in Figure 5.7c. The inductor current for mode 1 is given by

$$V_s = L\frac{di_1}{dt}$$

and is expressed as

$$i_1(t) = \frac{V_s}{L}t + I_1 \tag{5.28}$$

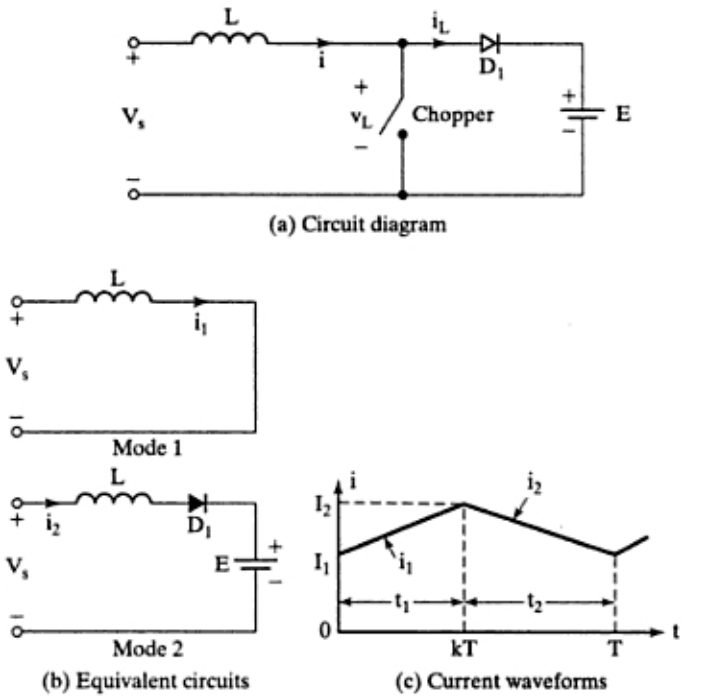


FIGURE 5.7
Arrangement for transfer of energy.

where I_1 is the initial current for mode 1. During mode 1, the current must rise and the necessary condition,

$$\frac{di_1}{dt} > 0 \quad \text{or} \quad V_s > 0$$

The current for mode 2 is given by

$$V_s = L\frac{di_2}{dt} + E$$

and is solved as

$$i_2(t) = \frac{V_s - E}{L}t + I_2 \tag{5.29}$$

where I_2 is initial current for mode 2. For a stable system, the current must fall and the condition is

$$\frac{di_2}{dt} < 0 \quad \text{or} \quad V_s < E$$

If this condition is not satisfied, the inductor current continues to rise and an unstable situation occurs. Therefore, the conditions for controllable power transfer are

$$0 < V_s < E \tag{5.30}$$

Equation (5.30) indicates that the source voltage V_s must be less than the voltage E to permit transfer of power from a fixed (or variable) source to a fixed dc voltage. In electric braking of dc motors, where the motors operate as dc generators, terminal voltage falls as the machine speed decreases. The converter permits transfer of power to a fixed dc source or a rheostat.

When the converter is turned on, the energy is transferred from the source V_s to inductor L. If the converter is then turned off, a magnitude of the energy stored in the inductor is forced to battery E.

Note: Without the chopping action, v_s must be greater than E for transferring power from V_s to E.

Key Points of Section 5.4

- A step-up dc converter can produce an output voltage that is higher than the input. The input current can be transferred to a voltage source higher than the input voltage.

5.5 STEP-UP CONVERTER WITH A RESISTIVE LOAD

A step-up converter with a resistive load is shown in Figure 5.8a. When switch S_1 is closed, the current rises through L and the switch. The equivalent circuit during mode 1 is shown in Figure 5.8b and the current is described by

$$V_s = L\frac{d}{dt}i_1$$

which for an initial current of I_1 gives

$$i_1(t) = \frac{V_s}{L}t + I_1 \tag{5.31}$$

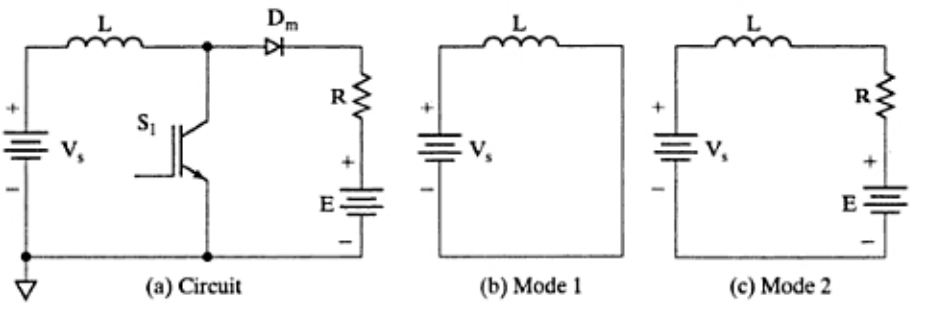


FIGURE 5.8
Step-up converter with a resistive load.

which is valid for $0 \le t \le kT$. At the end of mode 1 at $t = kT$,

$$I_2 = i_1(t = kT) = \frac{V_s}{L} kT + I_1 \tag{5.32}$$

When switch S_1 is opened, the inductor current flows through the RL load.

The equivalent current is shown in Figure 5.8c and the current during mode 2 is described by

$$V_s = Ri_2 + \frac{d}{dt} i_2 + E$$

which for an initial current of I_2 gives

$$i_2(t) = \frac{V_s - E}{L}\left(1 - e^{\frac{-tR}{L}}\right) + I_2 e^{\frac{-tR}{L}} \tag{5.33}$$

which is valid for $0 \le t \le (1 - k)T$. At the end of mode 2 at $t = (1 - k)T$.

$$I_1 = i_2[t = (1 - k)T] = \frac{V_s - E}{L}\left[1 - e^{-(1-k)z}\right] + I_2 e^{-(1-k)z} \tag{5.34}$$

where $z = TR/L$. Solving for I_1 and I_2 from Eqs. (5.32) and (5.34), we get

$$I_1 = \frac{V_s kz}{R} \frac{e^{-(1-k)z}}{1 - e^{-(1-k)z}} + \frac{V_s - E}{R} \tag{5.35}$$

$$I_2 = \frac{V_s kz}{R} \frac{1}{1 - e^{-(1-k)z}} + \frac{V_s - E}{R} \tag{5.36}$$

The ripple current is given by

$$\Delta I = I_2 - I_1 = \frac{V_s}{L} kT \tag{5.37}$$

These equations are valid for $E \le V_s$. If $E \ge V_s$ and the converter switch S_1 is opened, the inductor transfers its stored energy through R to the source and the inductor current is discontinuous.

Example 5.4 Finding the Currents of a Step-up Dc Converter

The step-up converter in Figure 5.8a has $V_s = 10\,V$, $f = 1$ kHz, $R = 5\,\Omega$, $L = 6.5$ mH, E = 0 V, and $k = 0.5$. Find I_1, I_2, and ΔI. Use SPICE to find these values and plot the load, diode, and switch current.

Solution

Equations (5.35) and (5.36) give $I_1 = 3.64$ A (3.36 A from SPICE) and $I_2 = 4.4$ A (4.15 A from SPICE). The plots of the load current $I(L)$, the diode current $I(D_m)$ and the switch current $IC(Q_1)$ are shown in Figure 5.9.

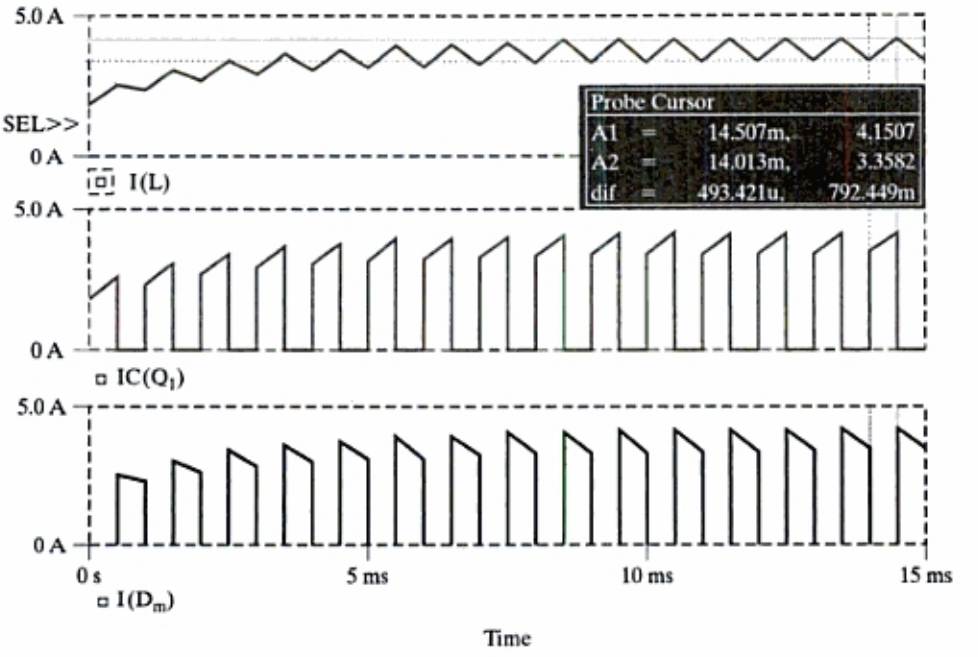


FIGURE 5.9

SPICE plots of load, input, and diode current for Example 5.4.

Key Points of Section 5.5

- With a resistive load, the load current and the voltage are pulsating. An output filter is required to smooth the output voltage.

5.6 PERFORMANCE PARAMETERS

The power semiconductor devices require a minimum time to turn on and turn off. Therefore, the duty cycle k can only be controlled between a minimum value k_{min} and a maximum value k_{max}, thereby limiting the minimum and maximum value of output voltage. The switching frequency of the converter is also limited. It can be noticed from Eq. (5.22) that the load ripple current depends inversely on the chopping frequency f. The frequency should be as high as possible to reduce the load ripple current and to minimize the size of any additional series inductor in the load circuit.

The performance parameters of the step-up and step-down converters are as follows:

Ripple current of the inductor, ΔI_L;

Maximum switching frequency, f_{max};

Condition for continuous or discontinuous inductor current;

Minimum value of inductor to maintain continuous inductor current;

Ripple content of the output voltage and output current, THD;
Ripple content of the input current, THD.

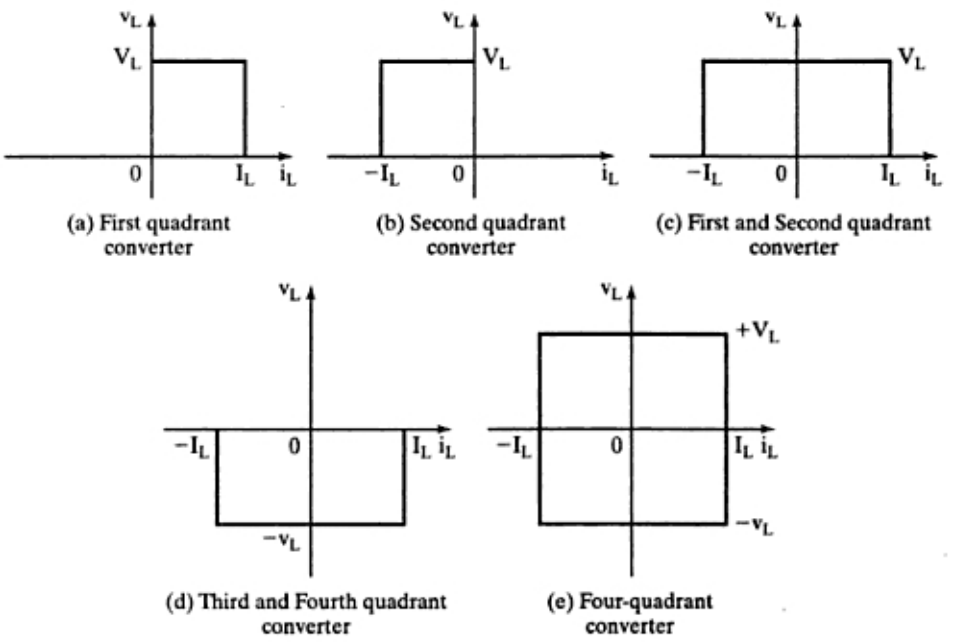
5.7 CONVERTER CLASSIFICATION

The step-down converter in Figure 5.1a only allows power to flow from the supply to the load, and is referred to as first quadrant converter. Depending on the directions of current and voltage flows, dc converters can be classified into five types:

1. First quadrant converter
2. Second quadrant converter
3. First and second quadrant converter
4. Third and fourth quadrant converter
5. Four-quadrant converter

First quadrant converter. The load current flows into the load. Both the load voltage and the load current are positive, as shown in Figure 5.10a. This is a single-quadrant converter and is said to be operated as a rectifier. Equations in Sections 5.2 and 5.3 can be applied to evaluate the performance of a first quadrant converter.

Second quadrant converter. The load current flows out of the load. The load voltage is positive, but the load current is negative, as shown in Figure 5.10b. This is also



(a) First quadrant converter
(b) Second quadrant converter
(c) First and Second quadrant converter
(d) Third and Fourth quadrant converter
(e) Four-quadrant converter

FIGURE 5.10
Dc converter classification.

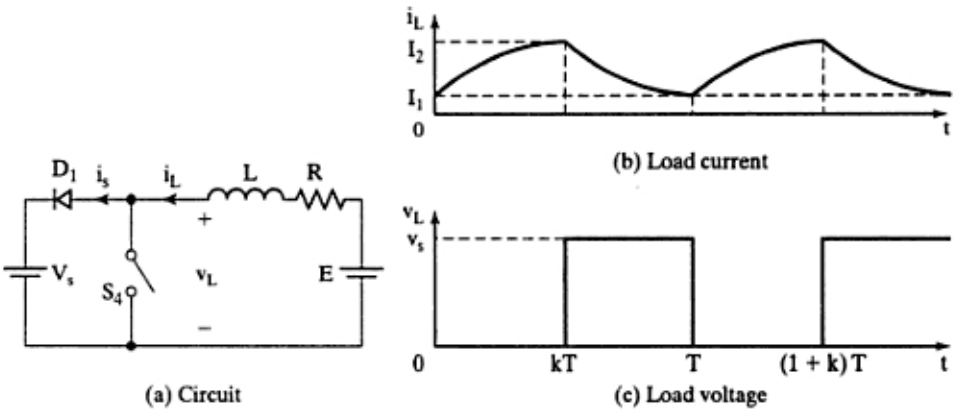


FIGURE 5.11

Second quadrant converter.

a single-quadrant converter, but operates in the second quadrant and is said to be operated as an inverter. A second quadrant converter is shown in Figure 5.11a, where the battery E is a part of the load and may be the back emf of a dc motor.

When switch S_4 is turned on, the voltage E drives current through inductor L and load voltage v_L becomes zero. The instantaneous load voltage v_L and load current i_L are shown in Figure 5.11b and 5.11c, respectively. The current i_L, which rises, is described by

$$0 = L\frac{di_L}{dt} + Ri_L + E$$

which, with initial condition $i_L(t = 0) = I_1$, gives

$$i_L = I_1 e^{-(R/L)t} - \frac{E}{R}(1 - e^{-(R/L)t}) \qquad \text{for } 0 \le t \le kT \tag{5.38}$$

At $t = t_1$,

$$i_L(t = t_1 = kT) = I_2 \tag{5.39}$$

When switch S_4 is turned off, a magnitude of the energy stored in inductor L is returned to the supply V_s via diode D_1. The load current i_L falls. Redefining the time origin $t = 0$, the load current i_L is described by

$$V_s = L\frac{di_L}{dt} + Ri_L + E$$

which, with initial condition $i(t = t_2) = I_2$, gives

$$i_L = I_2 e^{-(R/L)t} + \frac{V_s - E}{R}(1 - e^{-(R/L)t}) \qquad \text{for } 0 \le t \le t_2 \tag{5.40}$$

where $t_2 = (1 - k)T$. At $t = t_2$,

$$\begin{aligned} i_L(t = t_2) &= I_1 \quad \text{for steady-state continuous current} \\ &= 0 \quad \text{for steady-state discontinuous current} \end{aligned} \tag{5.41}$$

Using the boundary conditions in Eqs. (5.39) and (5.41), we can solve for I_1 and I_2 as

$$I_1 = \frac{V_S}{R}\left[\frac{1 - e^{-(1-k)z}}{1 - e^{-z}}\right] - \frac{E}{R} \tag{5.42}$$

$$I_2 = \frac{V_S}{R}\left(\frac{e^{-kz} - e^{-z}}{1 - e^{-z}}\right) - \frac{E}{R} \tag{5.43}$$

First and second quadrant converter. The load current is either positive or negative, as shown in Figure 5.10c. The load voltage is always positive. This is known as a *two-quadrant converter*. The first and second quadrant converters can be combined to form this converter, as shown in Figure 5.12. S_1 and D_4 operate as a first quadrant converter. S_2 and D_4 D_1 operate as a second quadrant converter. Care must be taken to ensure that the two switches are not fired together; otherwise, the supply V_s becomes short-circuited. This type of converter can operate either as a rectifier or as an inverter.

Third and fourth quadrant converter. The circuit is shown in Figure 5.13. The load voltage is always negative. The load current is either positive or negative, as

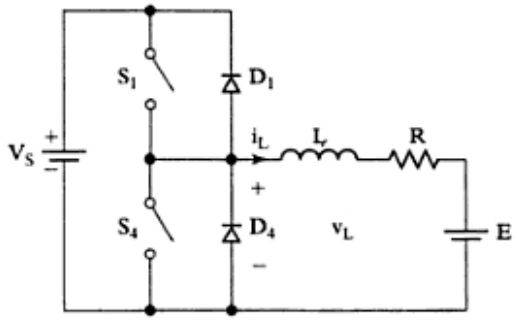


FIGURE 5.12
First and second quadrant converter.

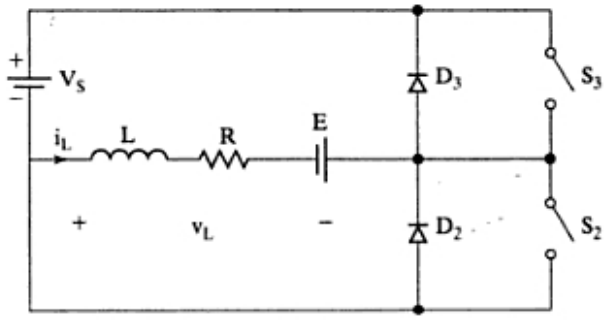


FIGURE 5.13
Third and fourth quadrant converter.

shown in Figure 5.10d. S_3 and D_2 operate to yield both a negative voltage and a load current. When S_3 is closed, a negative current flows through the load. When S_3 is opened, the load current freewheels through diode D_2. S_2 and D_3 operate to yield a negative voltage and a positive load current. When S_2 is closed, a positive load current flows. When S_2 is opened, the load current free wheels through diode D_3. It is important to note that the polarity of E must be reversed for this circuit to yield a negative voltage and a positive current. This is a negative two-quadrant converter. This converter can also operate as a rectifier or as an inverter.

Four-quadrant converter [2]. The load current is either positive or negative, as shown in Figure 5.10e. The load voltage is also either positive or negative. One first and second quadrant converter and one third and fourth quadrant converter can be combined to form the four-quadrant converter, as shown in Figure 5.14a. The polarities of the load voltage and load currents are shown in Figure 5.14b. The devices that are operative in different quadrants are shown in Figure 5.14c. For operation in the fourth quadrant, the direction of the battery E must be reversed. This converter forms the basis for the single-phase full-bridge inverter in Section 6.4.

For an inductive load with an emf (E) such as a dc motor, the four-quadrant converter can control the power flow and the motor speed in the forward direction (v_L positive and i_L positive), forward regenerative braking (v_L positive and i_L reverse), reverse direction (v_L negative and i_L reversing) and reverse regenerative braking (v_L negative and i_L negative).

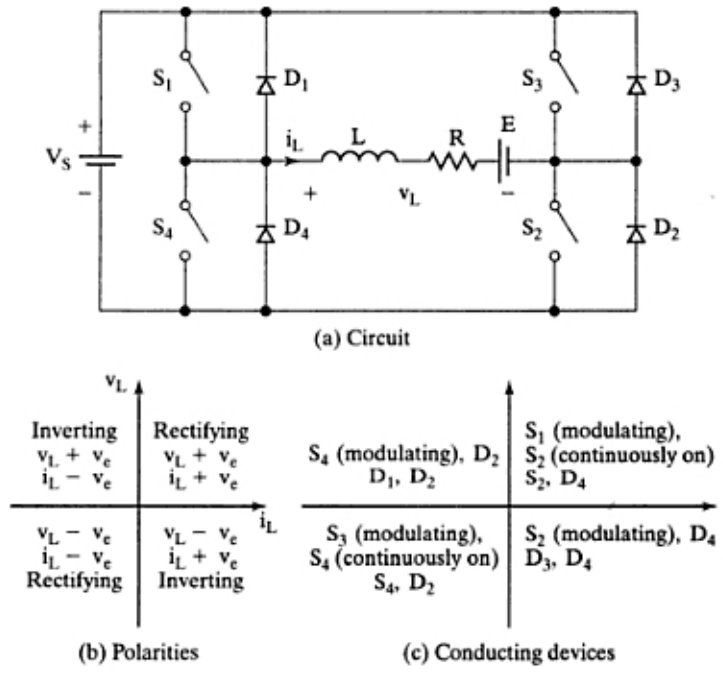


FIGURE 5.14
Four-quadrant converter.

Key Points of Section 5.7

- With proper switch control, the four-quadrant converter can operate and control flow in any of the four quadrants. For operation in the third and fourth quadrants, the direction of the load emf E must be reversed internally.

5.8 SWITCHING-MODE REGULATORS

Dc converters can be used as switching-mode regulators to convert a dc voltage, normally unregulated, to a regulated dc output voltage. The regulation is normally achieved by PWM at a fixed frequency and the switching device is normally BJT, MOSFET, or IGBT. The elements of switching-mode regulators are shown in Figure 5.15. We can notice from Figure 5.1b that the output of dc converters with resistive load is discontinuous and contains harmonics. The ripple content is normally reduced by an LC filter.

Switching regulators are commercially available as integrated circuits. The designer can select the switching frequency by choosing the values of R and C of frequency oscillator. As a rule of thumb, to maximize efficiency, the minimum oscillator period should be about 100 times longer than the transistor switching time; for example, if a transistor has a switching time of 0.5 μs, the oscillator period would be 50 μs, which gives the maximum oscillator frequency of 20 kHz. This limitation is due to a switching loss in the transistor. The transistor switching loss increases with the switching frequency and as a result the efficiency decreases. In addition, the core loss of inductors limits the high-frequency operation. Control voltage v_c is obtained by comparing the output voltage with its desired value. The v_{cr} can be compared with a sawtooth voltage v_r to generate the PWM control signal for the dc converter. There are four basic topologies of switching regulators [33, 34]:

1. Buck regulators
2. Boost regulators
3. Buck–boost regulators
4. Cúk regulators

5.8.1 Buck Regulators

In a buck regulator, the average output voltage V_a, is less than the input voltage, V_s—hence the name "buck," a very popular regulator [6, 7]. The circuit diagram of a buck

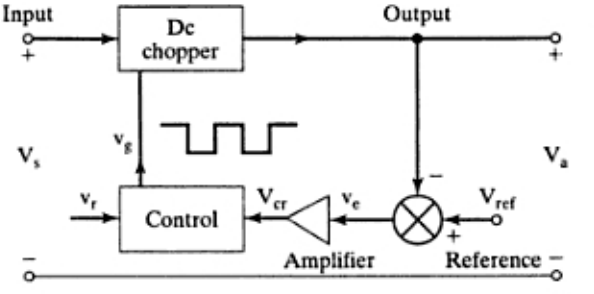


FIGURE 5.15
Elements of switching-mode regulators.

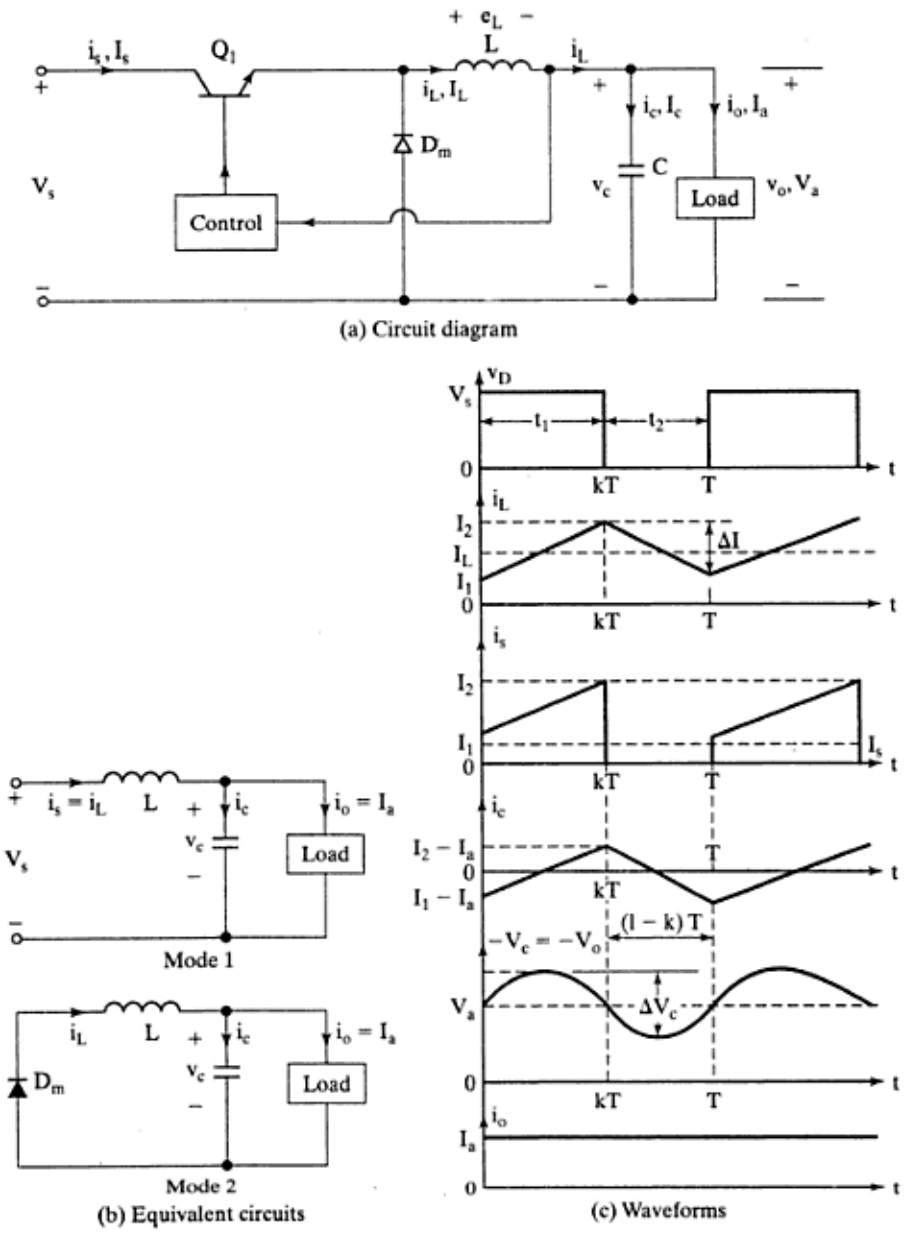


FIGURE 5.16

Buck regulator with continuous i_L.

regulator using a power BJT is shown in Figure 5.16a, and this is like a step-down converter. The circuit operation can be divided into two modes. Mode 1 begins when transistor Q_1 is switched on at $t = 0$. The input current, which rises, flows through filter inductor L, filter capacitor C, and load resistor R. Mode 2 begins when transistor Q_1 is switched off at $t = t_1$. The freewheeling diode D_m conducts due to energy stored in the

inductor; and the inductor current continues to flow through L, C, load, and diode D_m. The inductor current falls until transistor Q_1 is switched on again in the next cycle. The equivalent circuits for the modes of operation are shown in Figure 5.16b. The waveforms for the voltages and currents are shown in Figure 5.16c for a continuous current flow in the inductor L. It is assumed that the current rises and falls linearly. In practical circuits, the switch has a finite, nonlinear resistance. Its effect can generally be negligible in most applications. Depending on the switching frequency, filter inductance, and capacitance, the inductor current could be discontinuous.

The voltage across the inductor L is, in general,

$$e_L = L\frac{di}{dt}$$

Assuming that the inductor current rises linearly from I_1 to I_2 in time t_1,

$$V_s - V_a = L\frac{I_2 - I_1}{t_1} = L\frac{\Delta I}{t_1} \tag{5.44}$$

or

$$t_1 = \frac{\Delta I\, L}{V_s - V_a} \tag{5.45}$$

and the inductor current falls linearly from I_2 to I_1 in time t_2,

$$-V_a = -L\frac{\Delta I}{t_2} \tag{5.46}$$

or

$$t_2 = \frac{\Delta I\, L}{V_a} \tag{5.47}$$

where $\Delta I = I_2 - I_1$ is the peak-to-peak ripple current of the inductor L. Equating the value of ΔI in Eqs. (5.44) and (5.46) gives

$$\Delta I = \frac{(V_s - V_a)t_1}{L} = \frac{V_a t_2}{L}$$

Substituting $t_1 = kT$ and $t_2 = (1 - k)T$ yields the average output voltage as

$$V_a = V_s\frac{t_1}{T} = kV_s \tag{5.48}$$

Assuming a lossless circuit, $V_s I_s = V_a I_a = kV_s I_a$ and the average input current

$$I_s = kI_a \tag{5.49}$$

The switching period T can be expressed as

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta I\, L}{V_s - V_a} + \frac{\Delta I\, L}{V_a} = \frac{\Delta I\, LV_s}{V_a(V_s - V_a)} \tag{5.50}$$

which gives the peak-to-peak ripple current as

$$\Delta I = \frac{V_a(V_s - V_a)}{fLV_s} \tag{5.51}$$

or

$$\Delta I = \frac{V_s k(1 - k)}{fL} \tag{5.52}$$

Using Kirchhoff's current law, we can write the inductor current i_L as

$$i_L = i_c + i_o$$

If we assume that the load ripple current Δi_o is very small and negligible, $\Delta i_L = \Delta i_c$. The average capacitor current, which flows into for $t_1/2 + t_2/2 = T/2$, is

$$I_c = \frac{\Delta I}{4}$$

The capacitor voltage is expressed as

$$v_c = \frac{1}{C}\int i_c\, dt + v_c(t = 0)$$

and the peak-to-peak ripple voltage of the capacitor is

$$\Delta V_c = v_c - v_c(t = 0) = \frac{1}{C}\int_0^{T/2} \frac{\Delta I}{4}\, dt = \frac{\Delta I\, T}{8C} = \frac{\Delta I}{8fC} \tag{5.53}$$

Substituting the value of ΔI from Eq. (5.51) or (5.52) in Eq. (5.53) yields

$$\Delta V_c = \frac{V_a(V_s - V_a)}{8LCf^2V_s} \tag{5.54}$$

or

$$\Delta V_c = \frac{V_s k(1 - k)}{8LCf^2} \tag{5.55}$$

Condition for continuous inductor current and capacitor voltage. If I_L is the average inductor current, the inductor ripple current $\Delta I = 2I_L$.

Using Eqs. (5.48) and (5.52), we get

$$\frac{V_S(1 - k)k}{fL} = 2I_L = 2I_a = \frac{2kV_S}{R}$$

which gives the critical value of the inductor L_c as

$$L_c = L = \frac{(1 - k)R}{2f} \tag{5.56}$$

If V_c is the average capacitor voltage, the capacitor ripple voltage $\Delta V_c = 2V_a$. Using Eqs. (5.48) and (5.55), we get

$$\frac{V_S(1-k)k}{8LCf^2} = 2V_a = 2kV_S$$

which gives the critical value of the capacitor C_c as

$$C_c = C = \frac{1-k}{16Lf^2} \tag{5.57}$$

The buck regulator requires only one transistor, is simple, and has high efficiency greater than 90%. The *di/dt* of the load current is limited by inductor L. However, the input current is discontinuous and a smoothing input filter is normally required. It provides one polarity of output voltage and unidirectional output current. It requires a protection circuit in case of possible short circuit across the diode path.

Example 5.5 Finding the Values of *LC* Filter for the Buck Regulator

The buck regulator in Figure 5.16a has an input voltage of $V_s = 12$ V. The required average output voltage is $V_a = 5$ V at $R = 500\ \Omega$ and the peak-to-peak output ripple voltage is 20 mV. The switching frequency is 25 kHz. If the peak-to-peak ripple current of inductor is limited to 0.8 A, determine (a) the duty cycle k, (b) the filter inductance L, and (c) the filter capacitor C, and (d) the critical values of L and C.

Solution

$V_s = 12$ V, $\Delta V_c = 20$ mV, $\Delta I = 0.8$ A, $f = 25$ kHz, and $V_a = 5$ V.

a. From Eq. (5.48), $V_a = kV_s$ and $k = V_a/V_s = 5/12 = 0.4167 = 41.67\%$.

b. From Eq. (5.51),

$$L = \frac{5(12-5)}{0.8 \times 25{,}000 \times 12} = 145.83\ \mu\text{H}$$

c. From Eq. (5.53),

$$C = \frac{0.8}{8 \times 20 \times 10^{-3} \times 25{,}000} = 200\ \mu\text{F}$$

d. From Eq. (5.56), we get $L_c = \dfrac{(1-k)R}{2f} = \dfrac{(1-0.4167) \times 500}{2 \times 25 \times 10^3} = 5.83$ mH

From Eq. (5.57), we get $C_c = \dfrac{1-k}{16Lf^2} = \dfrac{1-0{,}4167}{16 \times 5.83 \times 10^2 \times (25 \times 10^3)^2} = 0.4\ \mu\text{F}$

5.8.2 Boost Regulators

In a boost regulator [8, 9] the output voltage is greater than the input voltage—hence the name "boost." A boost regulator using a power MOSFET is shown in Figure 5.17a. The circuit operation can be divided into two modes. Mode 1 begins when transistor

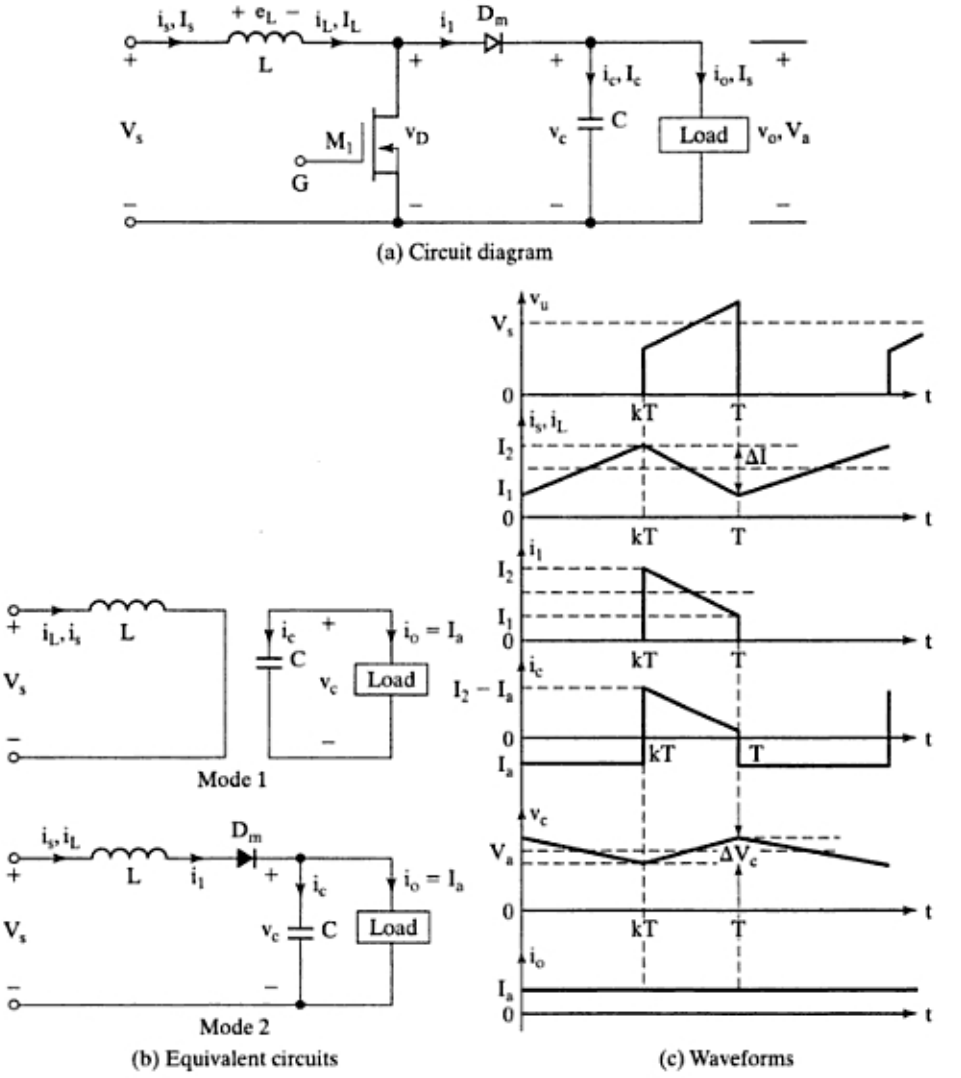


FIGURE 5.17

Boost regulator with continuous i_L.

M_1 is switched on at $t = 0$. The input current, which rises, flows through inductor L and transistor Q_1. Mode 2 begins when transistor M_1 is switched off at $t = t_1$. The current that was flowing through the transistor would now flow through L, C, load, and diode D_m. The inductor current falls until transistor M_1 is turned on again in the next cycle. The energy stored in inductor L is transferred to the load. The equivalent circuits for the modes of operation are shown in Figure 5.17b. The waveforms for voltages and currents are shown in Figure 5.17c for continuous load current, assuming that the current rises or falls linearly.

Assuming that the inductor current rises linearly from I_1 to I_2 in time t_1,

$$V_s = L\frac{I_2 - I_1}{t_1} = L\frac{\Delta I}{t_1} \tag{5.58}$$

or

$$t_1 = \frac{\Delta IL}{V_s} \tag{5.59}$$

and the inductor current falls linearly from I_2 to I_1 in time t_2,

$$V_s - V_a = -L\frac{\Delta I}{t_2} \tag{5.60}$$

or

$$t_2 = \frac{\Delta IL}{V_a - V_s} \tag{5.61}$$

where $\Delta I = I_2 - I_1$ is the peak-to-peak ripple current of inductor L. From Eqs. (5.58) and (5.60),

$$\Delta I = \frac{V_s t_1}{L} = \frac{(V_a - V_s)t_2}{L}$$

Substituting $t_1 = kT$ and $t_2 = (1 - k)T$ yields the average output voltage,

$$V_a = V_s\frac{T}{t_2} = \frac{V_s}{1 - k} \tag{5.62}$$

which gives

$$(1 - k) = \frac{V_S}{V_a} \tag{5.63}$$

Substituting $k = t_1/T = t_1 f$ into Eq. (5.63) yields

$$t_1 = \frac{V_a - V_S}{V_a f} \tag{5.64}$$

Assuming a lossless circuit, $V_s I_s = V_a I_a = V_s I_a/(1 - k)$ and the average input current is

$$I_s = \frac{I_a}{1 - k} \tag{5.65}$$

The switching period T can be found from

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta IL}{V_s} + \frac{\Delta IL}{V_a - V_s} = \frac{\Delta ILV_a}{V_s(V_a - V_s)} \tag{5.66}$$

and this gives the peak-to-peak ripple current:

$$\Delta I = \frac{V_s(V_a - V_s)}{fLV_a} \tag{5.67}$$

or

$$\Delta I = \frac{V_s k}{fL} \tag{5.68}$$

When the transistor is on, the capacitor supplies the load current for $t = t_1$. The average capacitor current during time t_1 is $I_c = I_a$ and the peak-to-peak ripple voltage of the capacitor is

$$\Delta V_c = v_c - v_c(t = 0) = \frac{1}{C}\int_0^{t_1} I_c\, dt = \frac{1}{C}\int_0^{t_1} I_a = \frac{I_a t_1}{C} \tag{5.69}$$

Substituting $t_1 = (V_a - V_s)/(V_a f)$ from Eq. (5.64) gives

$$\Delta V_c = \frac{I_a(V_a - V_s)}{V_a fC} \tag{5.70}$$

or

$$\Delta V_c = \frac{I_a k}{fC} \tag{5.71}$$

Condition for continuous inductor current and capacitor voltage. If I_L is the average inductor current, the inductor ripple current $\Delta I = 2I_L$.

Using Eqs. (5.62) and (5.68), we get

$$\frac{kV_S}{fL} = 2I_L = 2I_a = \frac{2V_S}{(1 - k)R}$$

which gives the critical value of the inductor L_c as

$$L_c = L = \frac{k(1 - k)R}{2f} \tag{5.72}$$

If V_c is the average capacitor voltage, the capacitor ripple voltage $\Delta V_c = 2V_a$. Using Eq. (5.71), we get

$$\frac{I_a k}{Cf} = 2V_a = 2I_a R$$

which gives the critical value of the capacitor C_c as

$$C_c = C = \frac{k}{2fR} \tag{5.73}$$

A boost regulator can step up the output voltage without a transformer. Due to a single transistor, it has a high efficiency. The input current is continuous. However, a high-peak current has to flow through the power transistor. The output voltage is very sensitive to changes in duty cycle k and it might be difficult to stabilize the regulator. The average output current is less than the average inductor current by a factor of $(1 - k)$, and a much higher rms current would flow through the filter capacitor, resulting in the use of a larger filter capacitor and a larger inductor than those of a buck regulator.

Example 5.6 Finding the Currents and Voltage in the Boost Regulator

A boost regulator in Figure 5.17a has an input voltage of $V_s = 5$ V. The average output voltage $V_a = 15$ V and the average load current $I_a = 0.5$ A. The switching frequency is 25 kHz. If $L = 150$ μH and $C = 220$ μF, determine (a) the duty cycle k, (b) the ripple current of inductor ΔI, (c) the peak current of inductor I_2, (d) the ripple voltage of filter capacitor ΔV_c, and (e) the critical values of L and C.

Solution

$V_s = 5$ V, $V_a = 15$ V, $f = 25$ kHz, $L = 150$ μH, and $C = 220$ μF.

a. From Eq. (5.62), $15 = 5/(1 - k)$ or $k = 2/3 = 0.6667 = 66.67\%$.

b. From Eq. (5.67),

$$\Delta I = \frac{5 \times (15 - 5)}{25{,}000 \times 150 \times 10^{-6} \times 15} = 0.89 \text{ A}$$

c. From Eq. (5.65), $I_s = 0.5/(1 - 0.667) = 1.5$ A and peak inductor current,

$$I_2 = I_s + \frac{\Delta I}{2} = 1.5 + \frac{0.89}{2} = 1.945 \text{ A}$$

d. From Eq. (5.71),

$$\Delta V_c = \frac{0.5 \times 0.6667}{25{,}000 \times 220 \times 10^{-6}} = 60.61 \text{ mV}$$

e. $R = \dfrac{V_a}{I_a} = \dfrac{15}{0.5} = 30\ \Omega$

From Eq. (5.72), we get $L_c = \dfrac{(1 - k)kR}{2f} = \dfrac{(1 - 0.6667) \times 0.6667 \times 30}{2 \times 25 \times 10^3} = 133$ μH

From Eq. (5.73), we get $C_c = \dfrac{k}{2fR} = \dfrac{0.6667}{2 \times 25 \times 10^3 \times 30} = 0.44$ μF

5.8.3 Buck–Boost Regulators

A buck–boost regulator provides an output voltage that may be less than or greater than the input voltage—hence the name "buck–boost"; the output voltage polarity is opposite to that of the input voltage. This regulator is also known as an *inverting regulator*. The circuit arrangement of a buck–boost regulator is shown in Figure 5.18a.

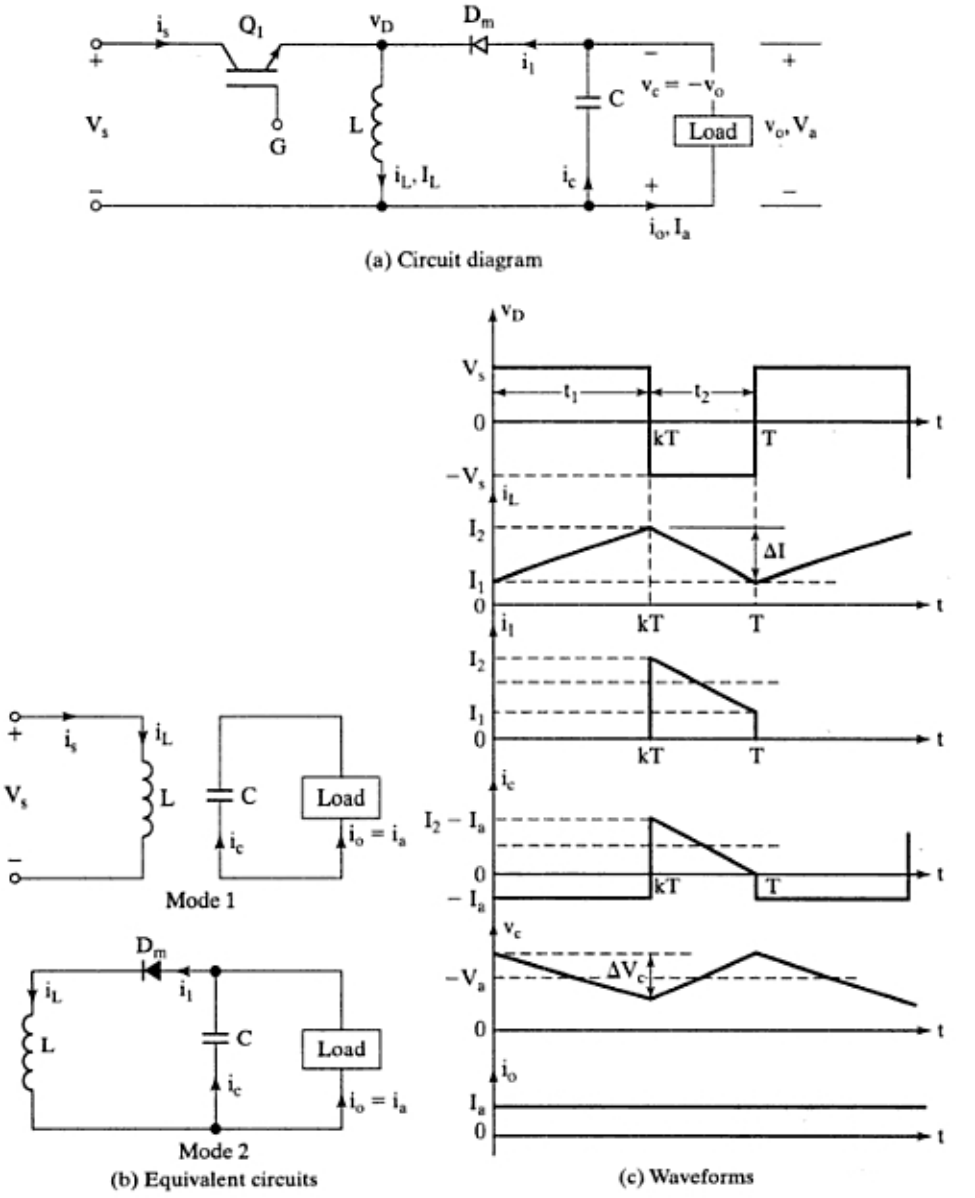


FIGURE 5.18

Buck–boost regulator with continuous i_L.

The circuit operation can be divided into two modes. During mode 1, transistor Q_1 is turned on and diode D_m is reversed biased. The input current, which rises, flows through inductor L and transistor Q_1. During mode 2, transistor Q_1 is switched off and the current, which was flowing through inductor L, would flow through L, C, D_m, and the load. The energy stored in inductor L would be transferred to the load and

the inductor current would fall until transistor Q_1 is switched on again in the next cycle. The equivalent circuits for the modes are shown in Figure 5.18b. The waveforms for steady-state voltages and currents of the buck–boost regulator are shown in Figure 5.18c for a continuous load current.

Assuming that the inductor current rises linearly from I_1 to I_2 in time t_1,

$$V_s = L\frac{I_2 - I_1}{t_1} = L\frac{\Delta I}{t_1} \tag{5.74}$$

or

$$t_1 = \frac{\Delta IL}{V_s} \tag{5.75}$$

and the inductor current falls linearly from I_2 to I_1 in time t_2,

$$V_a = -L\frac{\Delta I}{t_2} \tag{5.76}$$

or

$$t_2 = \frac{-\Delta IL}{V_a} \tag{5.77}$$

where $\Delta I = I_2 - I_1$ is the peak-to-peak ripple current of inductor L. From Eqs. (5.74) and (5.76),

$$\Delta I = \frac{V_s t_1}{L} = \frac{-V_a t_2}{L}$$

Substituting $t_1 = kT$ and $t_2 = (1 - k)T$, the average output voltage is

$$V_a = -\frac{V_s k}{1 - k} \tag{5.78}$$

Substituting $t_1 = kT$ and $t_2 = (1 - k)T$ into Eq. (5.78) yields

$$(1 - k) = \frac{-V_S}{V_a - V_S} \tag{5.79}$$

Substituting $t_2 = (1 - k)T$, and $(1 - k)$ from Eq. (5.79) into Eq. (5.78) yields

$$t_1 = \frac{V_a}{(V_a - V_S)f} \tag{5.80}$$

Assuming a lossless circuit, $V_s I_s = -V_a I_a = V_s I_a k/(1 - k)$ and the average input current I_s is related to the average output current I_a by

$$I_s = \frac{I_a k}{1 - k} \tag{5.81}$$

The switching period T can be found from

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta IL}{V_s} + \frac{\Delta IL}{V_a} = \frac{\Delta IL(V_a - V_s)}{V_s V_a} \tag{5.82}$$

and this gives the peak-to-peak ripple current,

$$\Delta I = \frac{V_s V_a}{fL(V_a - V_s)} \tag{5.83}$$

or

$$\Delta I = \frac{V_s k}{fL} \tag{5.84}$$

When transistor Q_1 is on, the filter capacitor supplies the load current for $t = t_1$. The average discharging current of the capacitor is $I_c = I_a$ and the peak-to-peak ripple voltage of the capacitor is

$$\Delta V_c = \frac{1}{C}\int_0^{t_1} I_c\, dt = \frac{1}{C}\int_0^{t_1} I_a\, dt = \frac{I_a t_1}{C} \tag{5.85}$$

Substituting $t_1 = V_a/[(V_a - V_s)f]$ from Eq. (5.80) becomes

$$\Delta V_c = \frac{I_a V_a}{(V_a - V_s)fC} \tag{5.86}$$

or

$$\Delta V_c = \frac{I_a k}{fC} \tag{5.87}$$

Condition for continuous inductor current and capacitor voltage. If I_L is the average inductor current, the inductor ripple current $\Delta I = 2I_L$. Using Eqs. (5.78) and (5.84), we get

$$\frac{kV_s}{fL} = 2I_L = 2I_a = \frac{2kV_s}{(1 - k)R}$$

which gives the critical value of the inductor L_c as

$$L_c = L = \frac{(1 - k)R}{2f} \tag{5.88}$$

If V_c is the average capacitor voltage, the capacitor ripple voltage $\Delta V_c = 2V_a$. Using Eq. (5.87), we get

$$\frac{I_a k}{Cf} = 2V_a = 2I_a R$$

which gives the critical value of the capacitor C_c as

$$C_c = C = \frac{k}{2fR} \tag{5.89}$$

A buck–boost regulator provides output voltage polarity reversal without a transformer. It has high efficiency. Under a fault condition of the transistor, the *di/dt* of the fault current is limited by the inductor L and will be V_s/L. Output short-circuit protection would be easy to implement. However, the input current is discontinuous and a high peak current flows through transistor Q_1.

Example 5.7 Finding the Currents and Voltage in the Buck–Boost Regulator

The buck–boost regulator in Figure 5.18a has an input voltage of $V_s = 12$ V. The duty cycle $k = 0.25$ and the switching frequency is 25 kHz. The inductance $L = 150$ μH and filter capacitance $C = 220$ μF. The average load current $I_a = 1.25$ A. Determine (a) the average output voltage, V_a; (b) the peak-to-peak output voltage ripple, ΔV_c; (c) the peak-to-peak ripple current of inductor, ΔI; (d) the peak current of the transistor, I_p; and (e) the critical values of L and C.

Solution

$V_s = 12$ V, $k = 0.25$, $I_a = 1.25$ A, $f = 25$ kHz, $L = 150$ μH, and $C = 220$ μF.

a. From Eq. (5.78), $V_a = -12 \times 0.25/(1 - 0.25) = -4$ V.

b. From Eq. (5.87), the peak-to-peak output ripple voltage is

$$\Delta V_c = \frac{1.25 \times 0.25}{25{,}000 \times 220 \times 10^{-6}} = 56.8 \text{ mV}$$

c. From Eq. (5.84), the peak-to-peak inductor ripple is

$$\Delta I = \frac{12 \times 0.25}{25{,}000 \times 150 \times 10^{-6}} = 0.8 \text{ A}$$

d. From Eq. (5.81), $I_s = 1.25 \times 0.25/(1 - 0.25) = 0.4167$ A. Because I_s is the average of duration kT, the peak-to-peak current of the transistor,

$$I_p = \frac{I_s}{k} + \frac{\Delta I}{2} = \frac{0.4167}{0.25} + \frac{0.8}{2} = 2.067 \text{ A}$$

e. $R = \dfrac{-V_a}{I_a} = \dfrac{4}{1.25} = 3.2\ \Omega$

From Eq. (5.88), we get $L_c = \dfrac{(1 - k)R}{2f} = \dfrac{(1 - 0.25) \times 3.2}{2 \times 25 \times 10^3} = 450$ μH.

From Eq. (5.89), we get $C_c = \dfrac{k}{2fR} = \dfrac{0.25}{2 \times 25 \times 10^3 \times 3.2} = 1.56$ μF.

5.8.4 Cúk Regulators

The circuit arrangement of the Cúk regulator [10] using a power bipolar junction transistor (BJT) is shown in Figure 5.19a. Similar to the buck–boost regulator, the Cúk regulator provides an output voltage that is less than or greater than the input voltage, but the output voltage polarity is opposite to that of the input voltage. It is named after its inventor [1]. When the input voltage is turned on and transistor Q_1 is switched off,

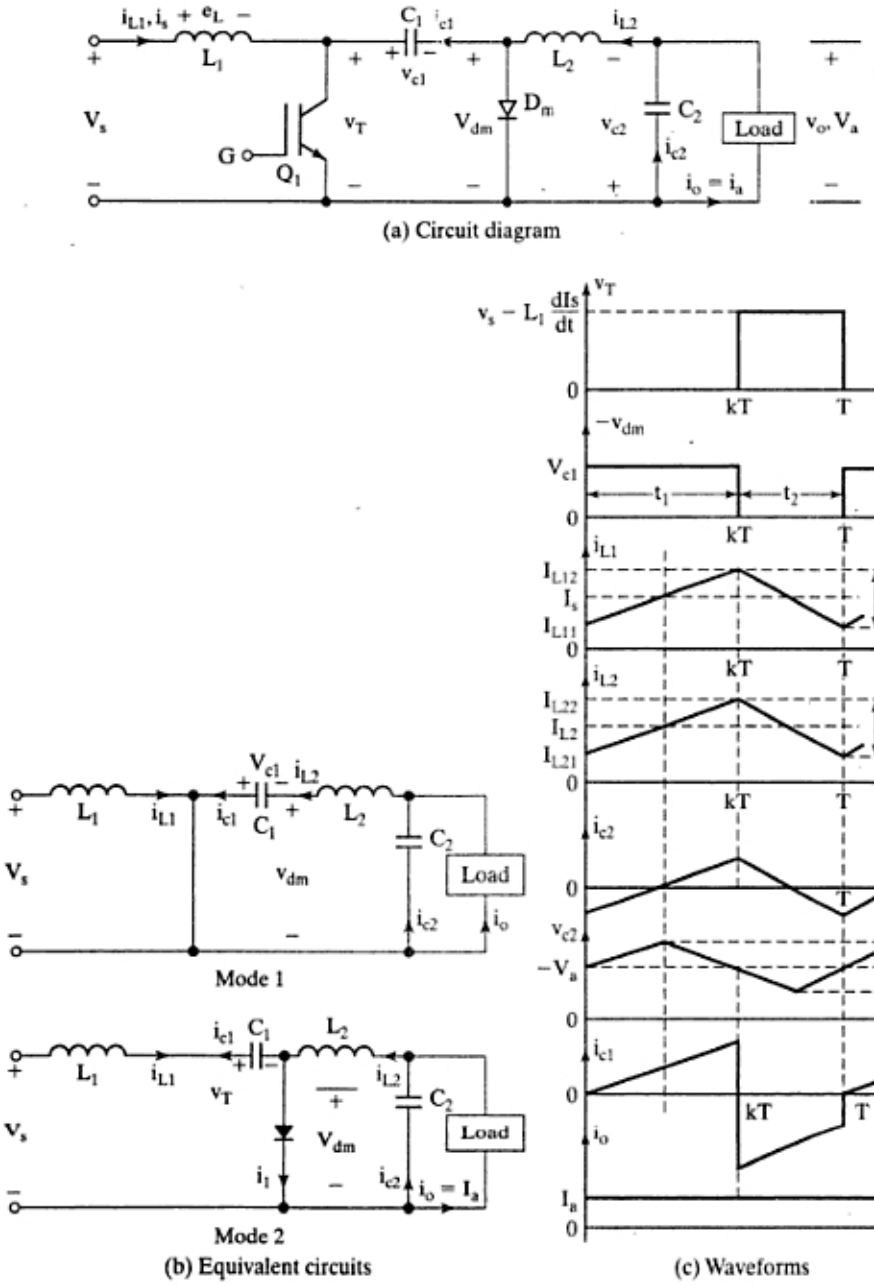


FIGURE 5.19

Cúk regulator.

diode D_m is forward biased and capacitor C_1 is charged through L_1, D_m, and the input supply V_s.

The circuit operation can be divided into two modes. Mode 1 begins when transistor Q_1 is turned on at $t = 0$. The current through inductor L_1 rises. At the same time, the voltage of capacitor C_1 reverse biases diode D_m and turns it off. The capacitor C_1 discharges its energy to the circuit formed by C_1, C_2, the load, and L_2. Mode 2 begins when transistor Q_1 is turned off at $t = t_1$. The capacitor C_1 is charged from the input supply and the energy stored in the inductor L_2 is transferred to the load. The diode D_m and transistor Q_1 provide a synchronous switching action. The capacitor C_1 is the medium for transferring energy from the source to the load. The equivalent circuits for the modes are shown in Figure 5.19b and the waveforms for steady-state voltages and currents are shown in Figure 5.19c for a continuous load current.

Assuming that the current of inductor L_1 rises linearly from I_{L11} to I_{L12} in time t_1,

$$V_s = L_1 \frac{I_{L12} - I_{L11}}{t_1} = L_1 \frac{\Delta I_1}{t_1} \tag{5.90}$$

or

$$t_1 = \frac{\Delta I_1 L_1}{V_s} \tag{5.91}$$

and due to the charged capacitor C_1, the current of inductor L_1 falls linearly from I_{L12} to I_{L11} in time t_2,

$$V_s - V_{c1} = -L_1 \frac{\Delta I_1}{t_2} \tag{5.92}$$

or

$$t_2 = \frac{-\Delta I_1 L_1}{V_s - V_{c1}} \tag{5.93}$$

where V_{c1} is the average voltage of capacitor C_1, and $\Delta I_1 = I_{L12} - I_{L11}$. From Eqs. (5.90) and (5.92).

$$\Delta I_1 = \frac{V_s t_1}{L_1} = \frac{-(V_s - V_{c1})t_2}{L_1}$$

Substituting $t_1 = kT$ and $t_2 = (1 - k)T$, the average voltage of capacitor C_1 is

$$V_{c1} = \frac{V_s}{1 - k} \tag{5.94}$$

Assuming that the current of filter inductor L_2 rises linearly from I_{L21} to I_{L22} in time t_1,

$$V_{c1} + V_a = L_2 \frac{I_{L22} - I_{L21}}{t_1} = L_2 \frac{\Delta I_2}{t_1} \tag{5.95}$$

or

$$t_1 = \frac{\Delta I_2 L_2}{V_{c1} + V_a} \tag{5.96}$$

and the current of inductor L_2 falls linearly from I_{L22} to I_{L21} in time t_2,

$$V_a = -L_2 \frac{\Delta I_2}{t_2} \tag{5.97}$$

or

$$t_2 = -\frac{\Delta I_2 L_2}{V_a} \tag{5.98}$$

where $\Delta I_2 = I_{L22} - I_{L21}$. From Eqs. (5.95) and (5.97),

$$\Delta I_2 = \frac{(V_{c1} + V_a)t_1}{L_2} = -\frac{V_a t_2}{L_2}$$

Substituting $t_1 = kT$ and $t_2 = (1 - k)T$, the average voltage of capacitor C_1 is

$$V_{c1} = -\frac{V_a}{k} \tag{5.99}$$

Equating Eq. (5.94) to Eq. (5.99), we can find the average output voltage as

$$V_a = -\frac{kV_s}{1 - k} \tag{5.100}$$

which gives

$$k = \frac{V_a}{V_a - V_S} \tag{5.101}$$

$$1 - k = \frac{V_S}{V_S - V_a} \tag{5.102}$$

Assuming a lossless circuit, $V_s I_s = -V_a I_a = V_s I_a k/(1 - k)$ and the average input current,

$$I_s = \frac{kI_a}{1 - k} \tag{5.103}$$

The switching period T can be found from Eqs. (5.91) and (5.93):

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta I_1 L_1}{V_s} - \frac{\Delta I_1 L_1}{V_s - V_{c1}} = \frac{-\Delta I_1 L_1 V_{c1}}{V_s(V_s - V_{c1})} \tag{5.104}$$

which gives the peak-to-peak ripple current of inductor L_1 as

$$\Delta I_1 = \frac{-V_s(V_s - V_{c1})}{f L_1 V_{c1}} \tag{5.105}$$

or

$$\Delta I_1 = \frac{V_s k}{f L_1} \tag{5.106}$$

The switching period T can also be found from Eqs. (5.96) and (5.98):

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta I_2 L_2}{V_{c1} + V_a} - \frac{\Delta I_2 L_2}{V_a} = \frac{-\Delta I_2 L_2 V_{c1}}{V_a(V_{c1} + V_a)} \tag{5.107}$$

and this gives the peak-to-peak ripple current of inductor L_2 as

$$\Delta I_2 = \frac{-V_a(V_{c1} + V_a)}{f L_2 V_{c1}} \tag{5.108}$$

or

$$\Delta I_2 = -\frac{V_a(1 - k)}{f L_2} = \frac{k V_s}{f L_2} \tag{5.109}$$

When transistor Q_1 is off, the energy transfer capacitor C_1 is charged by the input current for time $t = t_2$. The average charging current for C_1 is $I_{c1} = I_s$ and the peak-to-peak ripple voltage of the capacitor C_1 is

$$\Delta V_{c1} = \frac{1}{C_1}\int_0^{t_2} I_{c1}\, dt = \frac{1}{C_1}\int_0^{t_2} I_s\, dt = \frac{I_s t_2}{C_1} \tag{5.110}$$

Equation (5.102) gives $t_2 = V_s/[(V_s - V_a)f]$ and Eq. (5.110) becomes

$$\Delta V_{c1} = \frac{I_s V_s}{(V_s - V_a) f C_1} \tag{5.111}$$

or

$$\Delta V_{c1} = \frac{I_s(1 - k)}{f C_1} \tag{5.112}$$

If we assume that the load current ripple Δi_o is negligible, $\Delta i_{L2} = \Delta i_{c2}$. The average charging current of C_2, which flows for time $T/2$, is $I_{c2} = \Delta I_2/4$ and the peak-to-peak ripple voltage of capacitor C_2 is

$$\Delta V_{c2} = \frac{1}{C_2}\int_0^{T/2} I_{c2}\, dt = \frac{1}{C_2}\int_0^{T/2} \frac{\Delta I_2}{4}\, dt = \frac{\Delta I_2}{8 f C_2} \tag{5.113}$$

or

$$\Delta V_{c2} = -\frac{V_a(1 - k)}{8 C_2 L_2 f^2} = \frac{k V_s}{8 C_2 L_2 f^2} \tag{5.114}$$

Condition for continuous inductor current and capacitor voltage. If I_{L1} is the average current of inductor L_1, the inductor ripple current $\Delta I_1 = 2I_{L1}$. Using Eqs. (5.103) and (5.106), we get

$$\frac{kV_S}{fL_1} = 2I_{L1} = 2I_S = \frac{2kI_a}{1-k} = 2\left(\frac{k}{1-k}\right)^2\frac{V_S}{R}$$

which gives the critical value of the inductor L_{c1} as

$$L_{c1} = L_1 = \frac{(1-k)^2R}{2kf} \tag{5.115}$$

If I_{L2} is the average current of inductor L_2, the inductor ripple current $\Delta I_1 = 2I_{L2}$. Using Eqs. (5.100) and (5.109), we get

$$\frac{kV_S}{fL_2} = 2I_{L2} = 2I_a = \frac{2V_a}{R} = \frac{2kV_S}{(1-k)R}$$

which gives the critical value of the inductor L_{c2} as

$$L_{c2} = L_2 = \frac{(1-k)R}{2f} \tag{5.116}$$

If V_{c1} is the average capacitor voltage, the capacitor ripple voltage $\Delta V_{c1} = 2V_a$. Using $\Delta V_{c1} = 2\,V_a$ into Eq. (5.112), we get

$$\frac{I_S(1-k)}{fC_1} = 2V_a = 2I_aR$$

which, after substituting for I_S, gives the critical value of the capacitor C_{c1} as

$$C_{c1} = C_1 = \frac{k}{2fR} \tag{5.117}$$

If V_{c2} is the average capacitor voltage, the capacitor ripple voltage $\Delta V_{c2} = 2V_a$. Using Eq. (5.100) and (5.114), we get

$$\frac{kV_S}{8C_2L_2f^2} = 2V_a = \frac{2kV_S}{1-k}$$

which, after substituting for L_2 from Eq. (5.116), gives the critical value of the capacitor C_{c2} as

$$C_{c2} = C_2 = \frac{1}{8fR} \tag{5.118}$$

The Cúk regulator is based on the capacitor energy transfer. As a result, the input current is continuous. The circuit has low switching losses and has high efficiency. When transistor Q_1 is turned on, it has to carry the currents of inductors L_1 and L_2. As a result a high peak current flows through transistor Q_1. Because the capacitor provides

the energy transfer, the ripple current of the capacitor C_1 is also high. This circuit also requires an additional capacitor and inductor.

Example 5.8 Finding the Currents and Voltages in the Cúk Regulator

The input voltage of a Cúk converter in Figure 5.19a, $V_s = 12$ V. The duty cycle $k = 0.25$ and the switching frequency is 25 kHz. The filter inductance is $L_2 = 150\ \mu$H and filter capacitance is $C_2 = 220\ \mu$F. The energy transfer capacitance is $C_1 = 200\ \mu$F and inductance $L_1 = 180\ \mu$H. The average load current is $I_a = 1.25$ A. Determine (a) the average output voltage V_a; (b) the average input current I_s; (c) the peak-to-peak ripple current of inductor L_1, ΔI_1; (d) the peak-to-peak ripple voltage of capacitor C_1, ΔV_{c1}; (e) the peak-to-peak ripple current of inductor L_2, ΔI_2; (f) the peak-to-peak ripple voltage of capacitor C_2, ΔV_{c2}; and (g) the peak current of the transistor I_p.

Solution

$V_s = 12$ V, $k = 0.25$, $I_a = 1.25$ A, $f = 25$ kHz, $L_1 = 180\ \mu$H, $C_1 = 200\ \mu$F, $L_2 = 150\ \mu$H, and $C_2 = 220\ \mu$F.

a. From Eq. (5.100), $V_a = -0.25 \times 12/(1 - 0.25) = -4$ V.

b. From Eq. (5.103), $I_s = 1.25 \times 0.25/(1 - 0.25) = 0.42$ A.

c. From Eq. (5.106), $\Delta I_1 = 12 \times 0.25/(25{,}000 \times 180 \times 10^{-6}) = 0.67$ A.

d. From Eq. (5.112), $\Delta V_{c1} = 0.42 \times (1 - 0.25)/(25{,}000 \times 200 \times 10^{-6}) = 63$ mV.

e. From Eq. (5.109), $\Delta I_2 = 0.25 \times 12/(25{,}000 \times 150 \times 10^{-6}) = 0.8$ A.

f. From Eq. (5.113), $\Delta V_{c2} = 0.8/(8 \times 25{,}000 \times 220 \times 10^{-6}) = 18.18$ mV.

g. The average voltage across the diode can be found from

$$V_{dm} = -kV_{c1} = -V_a k \frac{1}{-k} = V_a \tag{5.119}$$

For a lossless circuit, $I_{L2}V_{dm} = V_a I_a$ and the average value of the current in inductor L_2 is

$$I_{L2} = \frac{I_a V_a}{V_{dm}} = I_a = 1.25 \text{ A} \tag{5.120}$$

Therefore, the peak current of transistor is

$$I_p = I_s + \frac{\Delta I_1}{2} + I_{L2} + \frac{\Delta I_2}{2} = 0.42 + \frac{0.67}{2} + 1.25 + \frac{0.8}{2} = 2.405 \text{ A}$$

5.8.5 Limitations of Single-Stage Conversion

The four regulators use only one transistor, employing only one stage conversion, and require inductors or capacitors for energy transfer. Due to the current-handling limitation of a single transistor, the output power of these regulators is small, typically tens of watts. At a higher current, the size of these components increases, with increased component losses, and the efficiency decreases. In addition, there is no isolation between the input and output voltage, which is a highly desirable criterion in most applications. For high-power applications, multistage conversions are used, where a dc voltage is

converted to ac by an inverter. The ac output is isolated by a transformer and then converted to dc by rectifiers. The multistage conversions are discussed in Section 14-4.

Key Points of Section 5.8

- A dc regulator can produce a dc output voltage, which is higher or lower than the dc supply voltage. *LC* filters are used to reduce the ripple content of the output voltage. Depending on the type of the regulator, the polarity of the output voltage can be opposite of the input voltage.

5.9 COMPARISON OF REGULATORS

When a current flows through an inductor, a magnetic field is set up. Any change in this current changes this field and an emf is induced. This emf acts in such a direction as to maintain the flux at its original density. This effect is known as the *self-induction*. An inductor limits the rise and fall of its currents and tries to maintain the ripple current low.

There is no change in the position of the main switch Q_1 for the buck and buck–boost regulators. Switch Q_1 is connected to the dc supply line. Similarly, there is no change in the position of the main switch Q_1 for the boost and Cúk regulators. Switch Q_1 is connected between the two supply lines. When the switch is closed, the supply is shorted through an inductor L, which limits the rate of rise of the supply current.

In Section 5.8, we derive the voltage gain of the regulators with the assumptions that there were no resistances associated with the inductors and capacitors. However, such resistances though small may reduce the gain significantly [11, 12]. Table 5.1 summarizes the voltage gains of the regulators.

Inductors and capacitors act as energy storage elements in switched-mode regulators, and as filter elements to smooth out the current harmonics. We can notice from Eqs. (B.17) and (B.18) in Appendix B that the magnetic loss increases with the square of frequency. On the other hand, a higher frequency reduces the size of inductors for

TABLE 5.1 Summaries of Regulator Gains [Ref. 11]

Regulator	Voltage Gain, $G(k) = V_o/V_S$ with Negligible Values of r_L and r_C	Voltage Gain, $G(k) = V_o/V_S$ with Finite Values of r_L and r_C
Buck	k	$\dfrac{kR}{R + r_L}$
Boost	$\dfrac{1}{1-k}$	$\dfrac{1}{1-k}\left[\dfrac{(1-k)^2R}{(1-k)^2R + r_L + k(1-k)\left(\dfrac{r_C R}{r_C + R}\right)}\right]$
Buck–boost	$\dfrac{-k}{1-k}$	$\dfrac{-k}{1-k}\left[\dfrac{(1-k)^2R}{(1-k)^2R + r_L + k(1-k)\left(\dfrac{r_C R}{r_C + R}\right)}\right]$

the same value of ripple current and filtering requirement. The design of dc–dc converters requires a compromise among switching frequency, inductor sizes, capacitor sizes, and switching losses.

5.10 MULTIOUTPUT BOOST CONVERTER

For a digital signal processor, high-speed computation requires a high supply voltage V_s for fast switching. Because power consumption is proportional to the square of V_s, it is advisable to lower V_s when lower computation speed is needed. A boost converter can be used to power high-speed processor cores with a very low supply voltage. A single-inductor dual-output (SIDO) boost converter topology [12] is shown in Figure 5.20.

The two outputs V_{oa} and V_{ob} share the inductor L and the switch S_1. Figure 5.21 shows the timing of the converter. It works with two complementary phases φ_a and φ_b. During $\varphi_a = 1$, S_b is opened and no current flows into V_{ob}, whereas S_1 is closed first. The inductor current I_L increases until the time $k_{1a}T$ expires (determined by the output of an error amplifier), where T is the switching period of the converter. During the time $k_{2a}T$, S_1 is opened and S_a is closed to divert the inductor current into the output V_{oa}. A zero current detector senses the inductor current, and when it goes to zero, the converter enters the time $k_{3a}T$, and S_a is opened again. The inductor current stays at zero until $\varphi_b = 1$. Thus, k_{1a}, k_{2a}, and k_{3a} must satisfy the requirements that

$$k_{1a} + k_{2a} \leq 0.5 \tag{5.121}$$

$$k_{1a} + k_{2a} + k_{3a} = 1 \tag{5.122}$$

During $\varphi_a = 1$, the controller multiplexes the inductor current into the output V_{oa} during $\varphi_a = 1$. Similarly, the controller multiplexes the inductor current into the output V_{ob} during $\varphi_b = 1$. The controller regulates the two outputs, alternately. Due to the presence of $k_{3a}T$ and $k_{3b}T$, the converter operates into the discontinuous conduction mode (DCM), essentially isolating the control of the two outputs such that load variation in one output does not affect the other. Therefore, the problem of cross regulation is alleviated. Another advantage of DCM control is simple compensation of the system

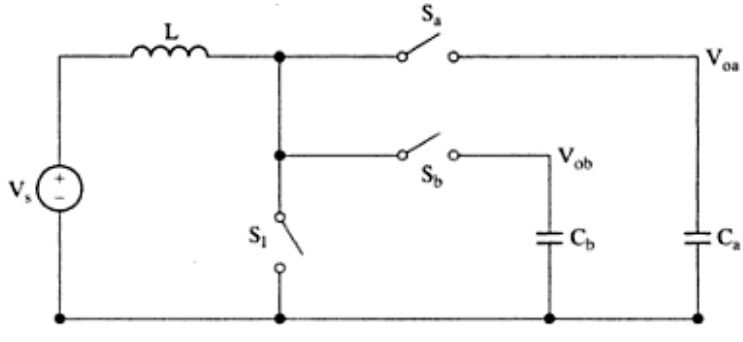


FIGURE 5.20

Single-inductor dual-output boost converter. [Ref. 12, D. Ma]

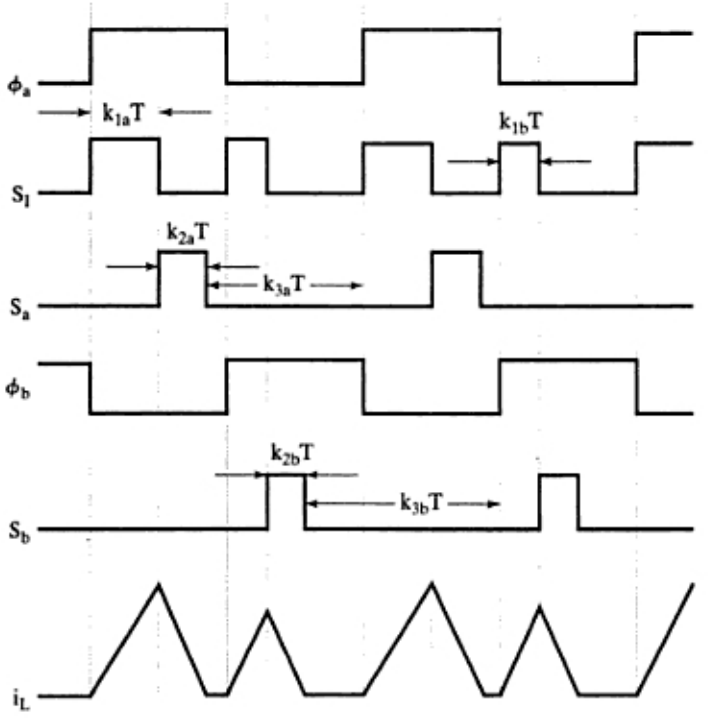


FIGURE 5.21

Timing diagram for the dual-output boost converter.

because there is only one LHP pole in the transfer function of the loop gain of each of the output [13].

With similar time multiplexing control, the dual-output converter can easily be extended to have N outputs as shown in Figure 5.22, if N nonoverlapping phases are assigned to the corresponding outputs accordingly. By employing time multiplexing (TM) control, a single controller is shared by all the outputs. Synchronous rectification, in the sense that the transistor in replacing the diode is switched off when the inductor current tends to go negative, is employed, thus eliminating diode drops and enhancing efficiency. All power switches and the controller can be fabricated on-chip [14, 15] and with only one inductor for all outputs, off-chip components are minimized.

Key Points of Section 5.10

- The boost converter can be extended to yield multiple outputs by using only a single inductor. By employing TM control, a single controller is shared by all the outputs. All power switches and the controller can be fabricated on-chip and with only one inductor for all outputs, off-chip components are minimized. This converter could find applications such as a power supply for high-speed digital signal processors.

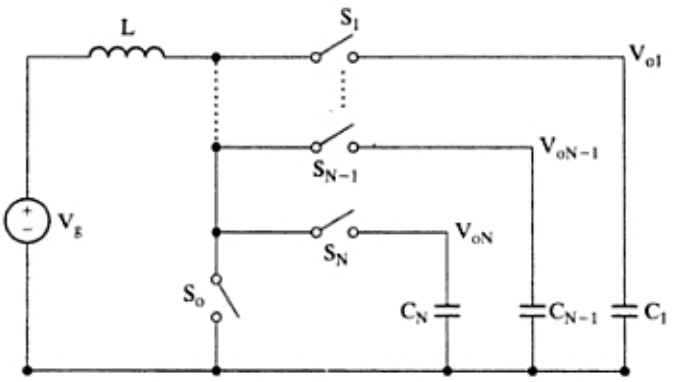


FIGURE 5.22

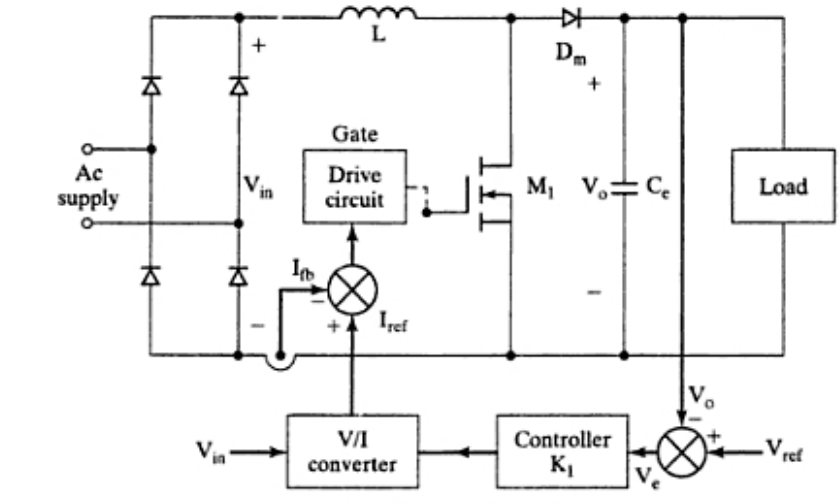
Topology of boost converter with N outputs.

5.11 DIODE RECTIFIER-FED BOOST CONVERTER

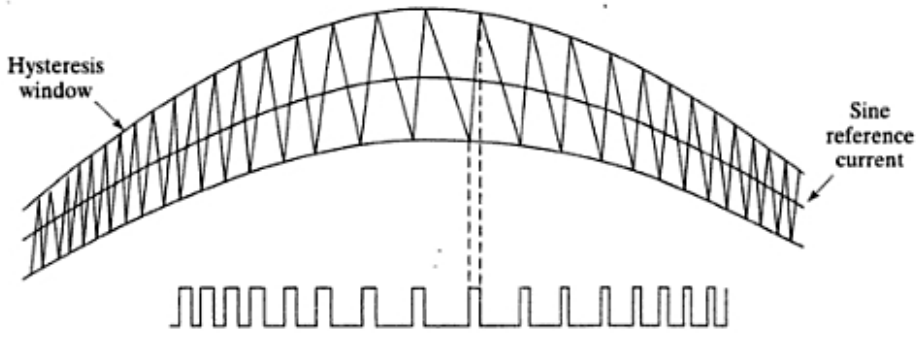
Diode rectifiers are the most commonly used circuits for applications where the input is the ac supply (e.g., in computers, telecommunications, fluorescent lighting, and air-conditioning). The power factor of diode rectifiers with a resistive load can be as high as 0.9, and it is lower with a reactive load. With the aid of a modern control technique, the input current of the rectifiers can be made sinusoidal and in phase with the input voltage, thereby having an input PF of approximate unity. A unity PF circuit that combines a full-bridge rectifier and a boost converter is shown in Figure 5.23a. The input current of the converter is controlled to follow the full-rectified waveform of the sinusoidal input voltage by PWM control [16–23]. The PWM control signals can be generated by using the bang–bang hysteresis (BBH) technique, similar to the delta modulation in Figure 6.26. This technique, which is shown in Figure 5.23b, has the advantage of yielding instantaneous current control, resulting in a fast response. However, the switching frequency is not constant and varies over a wide range during each half-cycle of the ac input voltage. The frequency is also sensitive to the values of the circuit components.

The switching frequency can be maintained constant by using the reference current I_{ref} and feedback current I_{fb} averaged over the per-switching period. This is shown in Figure 5.23c. I_{ref} is compared with I_{fb}. If $I_{ref} > I_{fb}$, the duty cycle is more than 50%. For $I_{ref} = I_{fb}$, the duty cycle is 50%. For $I_{ref} < I_{fb}$, the duty cycle is less than 50%. The error is forced to remain between the maximum and the minimum of the triangular waveform and the inductor current follows the reference sine wave, which is superimposed with a triangular waveform. The reference current I_{ref} is generated from the error voltage $V_e(= V_{ref} - V_o)$ and the input voltage V_{in} to the boost converter.

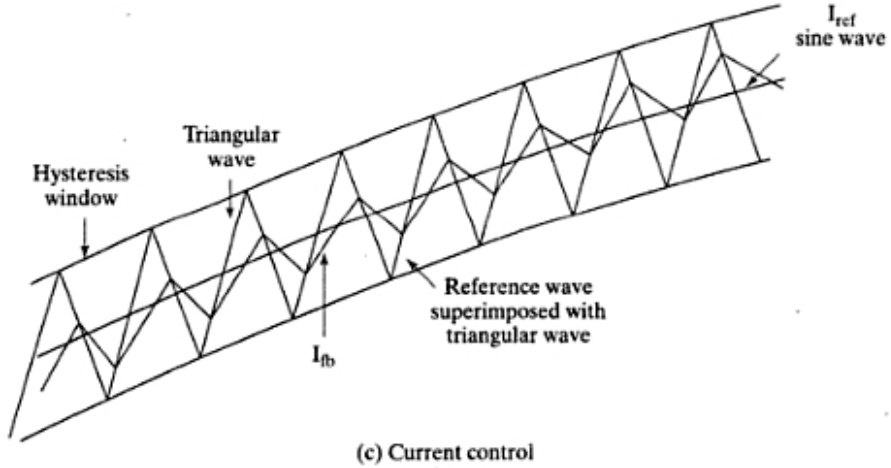
The boost converter can also be used for the power factor (PF) correction of three-phase diode rectifiers with capacitive output filters [19, 29] as shown in Figure 5.24. The boost converter is operated under DCM of the inductor current mode to achieve a sinusoidal input current shaping. This circuit uses only one active switch,



(a) Circuit arrangement



(b) Bang–bang hysteresis current control gate signals



(c) Current control

FIGURE 5.23

Power factor conditioning of diode rectifiers.

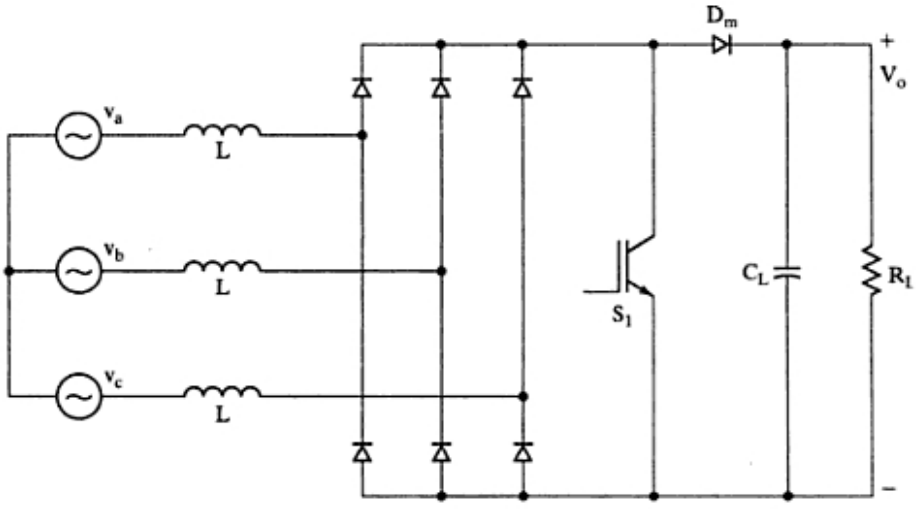


FIGURE 5.24

Three-phase rectifier-fed boost converter. [Ref. 29, C. Mufioz]

with no active control of the current. The drawbacks of the simple converter are excessive output voltage and the presence of fifth harmonics in the line current. This kind of converter is commonly used in industrial and commercial applications requiring a high input power factor because their input-current waveform automatically follows the input-voltage waveform. Also, the circuit has an extremely high efficiency.

However, if the circuit is implemented with the conventional constant-frequency, low-bandwidth, output-voltage feedback control, which keeps the duty cycle of the switch constant during a rectified line period, the rectifier input current exhibits a relatively large fifth-order harmonic. As a result, at power levels above 5 kW, the fifth-order harmonic imposes severe design, performance, and cost trade-offs to meet the maximum permissible harmonic current levels defined by the IEC555-2 document [30]. Advanced control methods such as the harmonic injection method [31] can reduce the fifth-order harmonic of the input current so that the power level at which the input current harmonic content still meets the IEC555-2 standard is extended.

Figure 5.25 shows the block diagram of the robust, harmonic injection technique introduced in [3–5]. A voltage signal that is proportional to the inverted ac component of the rectified, three-phase, line-to-line input voltages is injected into the output-voltage feedback loop. The injected signal varies the duty cycle of the rectifier within a line cycle to reduce the fifth-order harmonic and improve the THD of the rectifier input currents.

Key Points of Section 5.11

- The full-bridge rectifier can be combined with a boost converter to form a unity power factor circuit. By controlling the current of the boost inductor with the aid of feedback control technique, the input current of the rectifier can be made sinusoidal and in phase with the input voltage, thereby having an input PF of approximate unity.

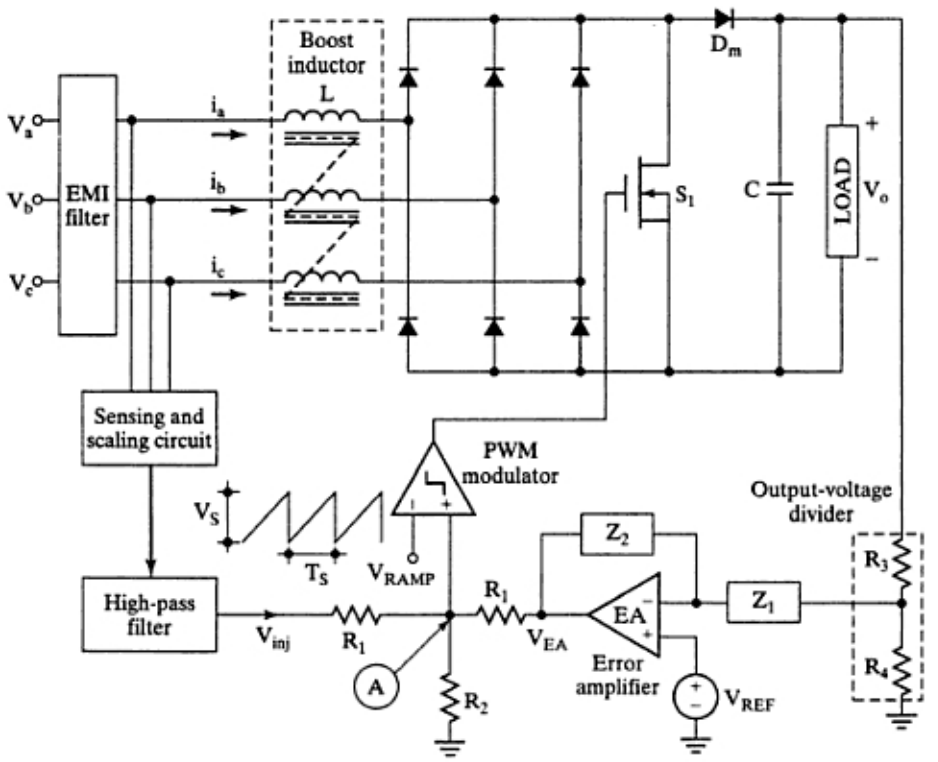


FIGURE 5.25

Three-phase DCM boost rectifier with a harmonic injection method. [Ref. 31, Y. Jang]

5.12 CHOPPER CIRCUIT DESIGN

We can notice from Eq. (5.7) that the output voltage contains harmonics. An output filter of C, LC, L type may be connected to the output to reduce the output harmonics [24, 25]. The techniques for filter design are similar to that of Examples 3.17 and 10.15.

A converter with a highly inductive load is shown in Figure 5.26a. The load current ripple is negligible ($\Delta I = 0$). If the average load current is I_a, the peak load current is $I_m = I_a + \Delta I = I_a$. The input current, which is of pulsed shape as shown in Figure 5.26b, contains harmonics and can be expressed in Fourier series as

$$i_{nh}(t) = kI_a + \frac{I_a}{n\pi}\sum_{n=1}^{\infty} \sin 2n\pi k \cos 2n\pi ft + \frac{I_a}{n\pi}\sum_{n=1}^{\infty}(1 - \cos 2n\pi k)\sin 2n\pi ft \tag{5.123}$$

The fundamental component ($n = 1$) of the converter-generated harmonic current at the input side is given by

$$i_{1h}(t) = \frac{I_a}{\pi}\sin 2\pi k \cos 2\pi ft + \frac{I_a}{\pi}(1 - \cos 2\pi k)\sin 2\pi ft \tag{5.124}$$

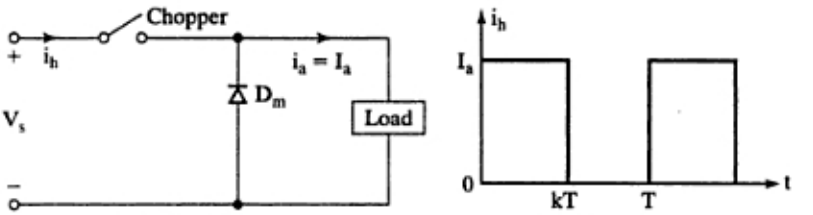


FIGURE 5.26
Input current waveform of converter.

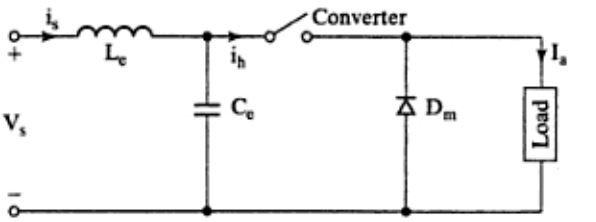


FIGURE 5.27
Converter with input filter.

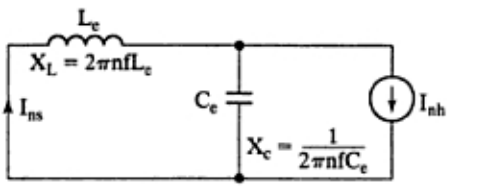


FIGURE 5.28
Equivalent circuit for harmonic currents.

In practice, an input filter as shown in Figure 5.27 is normally connected to filter out the converter-generated harmonics from the supply line. The equivalent circuit for the converter-generated harmonic currents is shown in Figure 5.28, and the rms value of the nth harmonic component in the supply can be calculated from

$$I_{ns} = \frac{1}{1 + (2n\pi f)^2 L_e C_e} I_{nh} = \frac{1}{1 + (nf/f_0)^2} I_{nh} \tag{5.125}$$

where f is the chopping frequency and $f_0 = 1/(2\pi\sqrt{L_e C_e})$ is the filter resonant frequency. If $(f/f_0) \gg 1$, which is generally the case, the nth harmonic current in the supply becomes

$$I_{ns} = I_{nh}\left(\frac{f_0}{nf}\right)^2 \tag{5.126}$$

A high chopping frequency reduces the sizes of input filter elements, but the frequencies of converter-generated harmonics in the supply line are also increased; and this may cause interference problems with control and communication signals.

If the source has some inductances, L_s, and the converter switch as in Figure 5.1a is turned on, an amount of energy can be stored in the source inductance. If an attempt

is made to turn off the converter switch, the power semiconductor devices might be damaged due to an induced voltage resulting from this stored energy. The LC input filter provides a low-impedance source for the converter action.

Example 5.9 Finding the Harmonic Input Current of a Dc Converter

A highly inductive load is supplied by a converter as shown in Figure 5.26a. The average load current is $I_a = 100$ A and the load ripple current can be considered negligible ($\Delta I = 0$). A simple LC input filter with $L_e = 0.3$ mH and $C_e = 4500$ μF is used. If the converter is operated at a frequency of 350 Hz and a duty cycle of 0.5, determine the maximum rms value of the fundamental component of converter-generated harmonic current in the supply line.

Solution

For $I_a = 100$ A, $f = 350$ Hz, $k = 0.50$, $C_e = 4500$ μF, and $L_e = 0.3$ mH, $f_0 = 1/(2\pi\sqrt{C_eL_e}) = 136.98$ Hz. Equation (5.124) can be written as

$$I_{1h}(t) = A_1 \cos 2\pi ft + B_1 \sin 2\pi ft$$

where $A_1 = (I_a/\pi) \sin 2\pi k$ and $B_1 = (I_a/\pi)(1 - \cos 2\pi k)$. The peak magnitude of this current is calculated from

$$I_{ph} = (A_1^2 + B_1^2)^{1/2} = \frac{\sqrt{2}I_a}{\pi}(1 - \cos 2\pi k)^{1/2} \tag{5.127}$$

The rms value of this current is

$$I_{1h} = \frac{I_a}{\pi}(1 - \cos 2\pi k)^{1/2} = 45.02 \text{ A}$$

and this becomes maximum at $k = 0.5$. The fundamental component of converter-generated harmonic current in the supply can be calculated from Eq. (5.125) and is given by

$$I_{1s} = \frac{1}{1 + (f/f_0)^2} I_{1h} = \frac{45.02}{1 + (350/136.98)^2} = 5.98 \text{ A}$$

If $f/f_0 \gg 1$, the harmonic current in the supply becomes approximately

$$I_{1s} = I_{1h}\left(\frac{f_0}{f}\right)^2$$

Key Points of Section 5.12

- The design of a dc–dc converter circuit requires (a) determining the converter topology, (b) finding the voltage and currents of the switching devices, (c) finding the values and ratings of passive elements such as capacitors and inductors, and (d) choosing the control strategy and the gating algorithm in order to obtain the desired output.

Example 5.10

A buck converter is shown in Figure 5.29. The input voltage is $V_s = 110$ V, the average load voltage is $V_a = 60$ V, and the average load current is $I_a = 20$ A. The chopping frequency is $f = 20$ kHz. The peak-to-peak ripples are 2.5% for load voltage, 5% for load current, and 10% for filter L_e current. (a) Determine the values of L_e, L, and C_e. Use PSpice (b) to verify the results by plotting the instantaneous capacitor voltage v_C, and instantaneous load current i_L; and (c) to calculate the Fourier coefficients and the input current i_S. The SPICE model parameters of the transistor are IS = 6.734f, BF = 416.4, BR = 0.7371, CJC = 3.638P, CJE = 4.493P, TR = 239.5N, TF = 301.2P, and that of the diode are IS = 2.2E−15, BV = 1800V, TT = 0.

Solution

$$V_s = 110\text{ V}, V_a = 60\text{ V}, I_a = 20\text{ A}.$$
$$\Delta V_c = 0.025 \times V_a = 0.025 \times 60 = 1.5\text{ V}$$
$$R = \frac{V_a}{I_a} = \frac{60}{20} = 3\ \Omega$$

From Eq. (5.48),

$$k = \frac{V_a}{V_s} = \frac{60}{110} = 0.5455$$

From Eq. (5.49),

$$I_s = kI_a = 0.5455 \times 20 = 10.91\text{ A}$$
$$\Delta I_L = 0.05 \times I_a = 0.05 \times 20 = 1\text{ A}$$
$$\Delta I = 0.1 \times I_a = 0.1 \times 20 = 2\text{ A}$$

a. From Eq. (5.51), we get the value of L_e:

$$L_e = \frac{V_a(V_s - V_a)}{\Delta I f V_s} = \frac{60 \times (110 - 60)}{2 \times 20\text{ kHz} \times 110} = 681.82\ \mu\text{H}$$

From Eq. (5.53) we get the value of C_e:

$$C_e = \frac{\Delta I}{\Delta V_c \times 8f} = \frac{2}{1.5 \times 8 \times 20\text{ kHz}} = 8.33\ \mu\text{F}$$

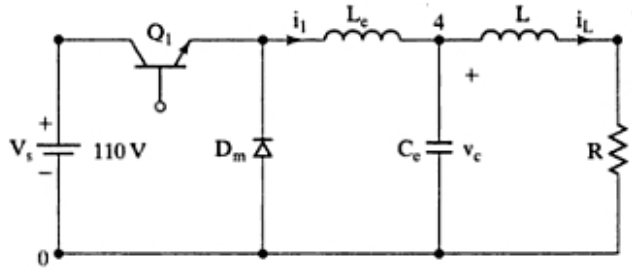


FIGURE 5.29
Buck converter.

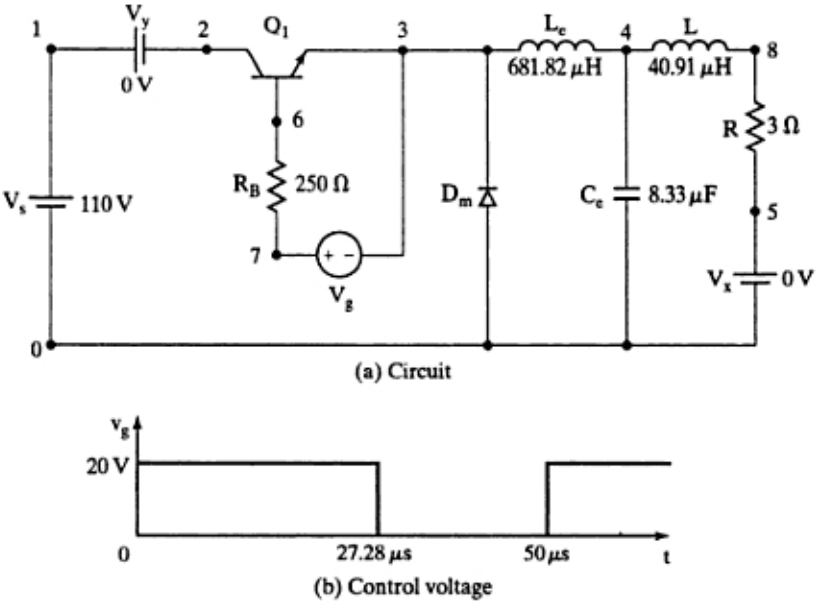


FIGURE 5.30

Buck chopper for PSpice simulation.

Assuming a linear rise of load current i_L during the time from $t = 0$ to $t_1 = kT$, we can write approximately

$$L\frac{\Delta I_L}{t_1} = L\frac{\Delta I_L}{kT} = \Delta V_C$$

which gives the approximate value of L:

$$\begin{aligned} L &= \frac{kT\Delta V_c}{\Delta I_L} = \frac{k\Delta V_c}{\Delta I_L f} \\ &= \frac{0.5454 \times 1.5}{1 \times 20\,\text{kHz}} = 40.91\ \mu\text{H} \end{aligned} \tag{5.128}$$

b. $k = 0.5455$, $f = 20$ kHz, $T = 1/f = 50\ \mu$s, and $t_{on} = k \times T = 27.28\ \mu$s. The buck chopper for PSpice simulation is shown in Figure 5.30a. The control voltage V_g is shown in Figure 5.30b. The list of the circuit file is as follows:

```
Example 5.10     Buck Converter
VS    1    0     DC    110V
VY    1    2     DC    0V    ; Voltage source to measure input current
Vg    7    3     PULSE (0V  20V  0  0.1NS  0.1NS  27.28US 50US)
RB    7    6     250                          ; Transistor base resistance
LE    3    4     681.82UH
```

```
CE    4    0     8.33UF      IC=60V  ;  initial voltage
L     4    8     40.91UH
R     8    5     3
VX    5    0     DC    0V            ; Voltage source to measure load current
DM    0    3     DMOD                ; Freewheeling diode
.MODEL   DMOD    D(IS=2.2E-15 BV=1800V TT=0)     ; Diode model parameters
Q1    2    6     3     QMOD          ; BJT switch
.MODEL  QMOD  NPN  (IS=6.734F BF=416.4 BR=.7371 CJC=3.638P
+ CJE=4.493P TR=239.5N TF=301.2P)    ; BJT model parameters
.TRAN  1US 1.6MS 1.5MS 1US  UIC      ; Transient analysis
.PROBE                               ; Graphics postprocessor
.options  abstol = 1.00n reltol = 0.01 vntol = 0.1 ITL5=50000 ; convergence
.FOUR   20KHZ   I(VY)                ; Fourier analysis
.END
```

The PSpice plots are shown in Figure 5.31, where $I(VX)$ = load current, $I(Le)$ = inductor L_e current, and $V(4)$ = capacitor voltage. Using the PSpice cursor in Figure 5.31 gives $V_a = V_c = 59.462$ V, $\Delta V_c = 1.782$ V, $\Delta I = 2.029$ A, $I_{(av)} = 19.813$ A, $\Delta I_L = 0.3278$ A, and $I_a = 19.8249$ A. This verifies the design; however, ΔI_L gives a better result than expected.

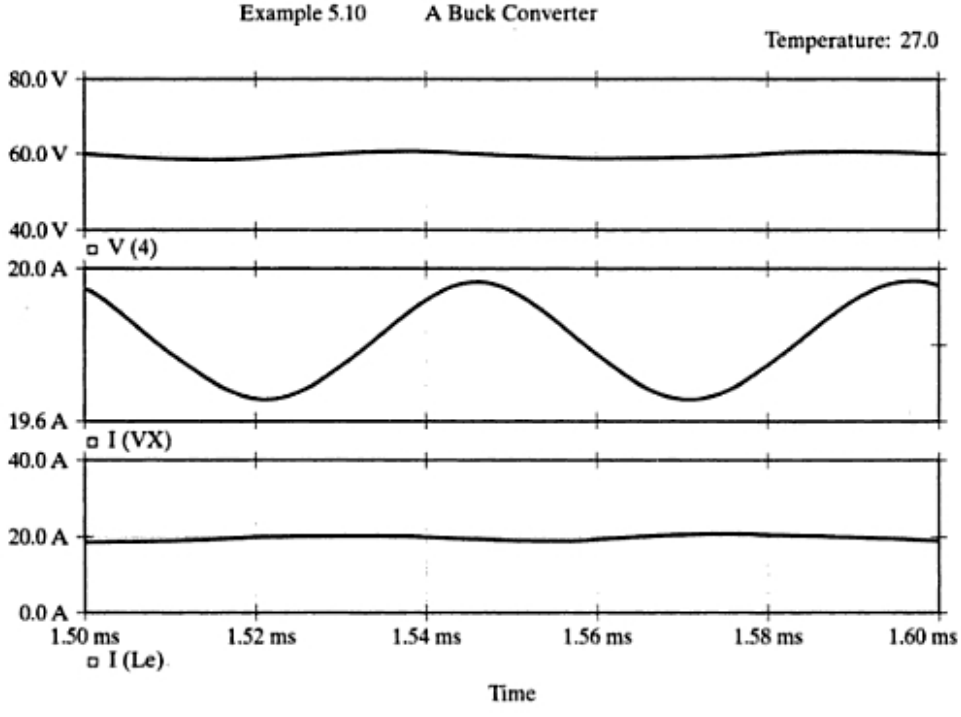


FIGURE 5.31

PSpice plots for Example 5.10.

c. The Fourier coefficients of the input current are

FOURIER COMPONENTS OF TRANSIENT RESPONSE I(VY)

DC COMPONENT = 1.079535E+01

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	2.000E+04	1.251E+01	1.000E+00	−1.195E+01	0.000E+00
2	4.000E+04	1.769E+00	1.415E-01	7.969E+01	9.163E+01
3	6.000E+04	3.848E+00	3.076E-01	−3.131E+01	−1.937E+01
4	8.000E+04	1.686E+00	1.348E-01	5.500E+01	6.695E+01
5	1.000E+05	1.939E+00	1.551E-01	−5.187E+01	−3.992E+01
6	1.200E+05	1.577E+00	1.261E-01	3.347E+01	4.542E+01
7	1.400E+05	1.014E+00	8.107E-02	−7.328E+01	−6.133E+01
8	1.600E+05	1.435E+00	1.147E-01	1.271E+01	2.466E+01
9	1.800E+05	4.385E-01	3.506E-02	−9.751E+01	−8.556E+01

TOTAL HARMONIC DISTORTION = 4.401661E+01 PERCENT

Key Points of Section 5.12

- The design of a dc–dc converter circuit requires (1) determining the converter topology, (2) finding the voltage and currents of the switching devices, (3) finding the values and ratings of passive elements such as capacitors and inductors, and (4) choosing the control strategy and the gating algorithm to obtain the desired output.

5.13 STATE–SPACE ANALYSIS OF REGULATORS

Any nth order linear or nonlinear differential equation in one time-dependent variable can be written [26] as n first-order differential equation in n time-dependent variables x_1 through x_n. Let us consider, for example, the following third-order equation:

$$y''' + a_2 y'' + a_1 y' + a_0 = 0 \tag{5.129}$$

where y' is the first derivative of y, $y' = (d/dt)\,y$. Let y be x_1. Then Eq. (5.129) can be represented by the three equations

$$x_1' = x_2 \tag{5.130}$$

$$x_2'' = x_3 \tag{5.131}$$

$$x_3'' = -a_0 x_1 - a_1 x_2 - a_3 x_3 \tag{5.132}$$

In each case, n initial conditions must be known before an exact solution can be found. For any nth-order system, a set of n-independent variables is necessary and sufficient to describe that system completely. These variables $x_1, x_2, \ldots, x_n$. are called the *state variables* for the system. If the initial conditions of a linear system are known at time t_0, then we can find the states of the systems for all time $t > t_0$ and for a given set of input sources.

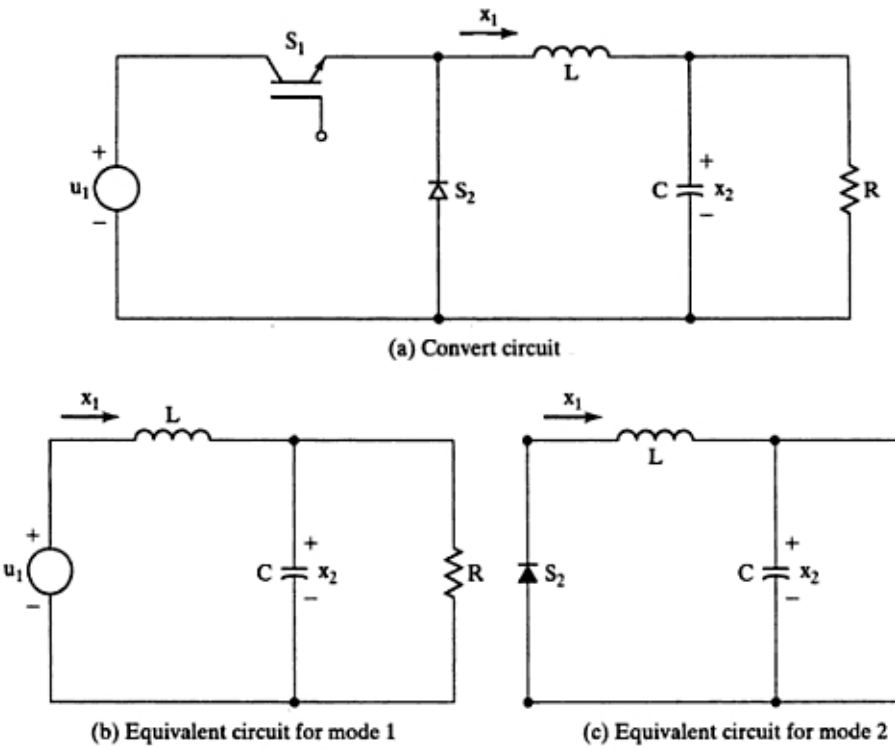


FIGURE 5.32

Buck converter with state variables.

All state variables are subscribed x's and all sources are subscribed u's. Let us consider the basic buck converter of Figure 5.16a, which is redrawn in Figure 5.32a. The dc source V_s is replaced with the more general source u_1.

Mode 1. Switch S_1 is on and switch S_2 is off. The equivalent circuit is shown in Figure 5.32b. Applying Kirchoff's voltage law (KVL), we get

$$u_1 = Lx_1' + x_2$$

$$Cx_2' = x_1 - \frac{1}{R}x_2$$

which can be rearranged to

$$x_1' = \frac{-1}{L}x_2 + \frac{1}{L}u_1 \tag{5.133}$$

$$x_2' = \frac{-1}{C}x_2 + \frac{1}{RC}x_2 \tag{5.134}$$

These equations can be written in the universal format:

$$x' = A_1 x + B_1 u_1 \tag{5.135}$$

where $\mathbf{x}$ = state vector = $\begin{pmatrix} \mathbf{x}_1 \\ \mathbf{x}_2 \end{pmatrix}$

A_1 = state coefficient matrix = $\begin{pmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{pmatrix}$

$\mathbf{u}_1$ = source vector

B_1 = source coefficient matrix = $\begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix}$

Mode 2. Switch S_1 is off and switch S_2 is on. The equivalent circuit is shown in Figure 5-32c. Applying KVL, we get

$$0 = Lx_1' + x_2$$

$$Cx_2' = x_1 - \frac{1}{R} x_2$$

which can be rearranged to

$$x_1' = \frac{-1}{L} x_2 \tag{5.136}$$

$$x_2' = \frac{-1}{C} x_2 + \frac{1}{RC} x_2 \tag{5.137}$$

These equations can be written in the universal format:

$$x' = A_2 x + B_2 u_1 \tag{5.138}$$

where $\mathbf{x}$ = state vector = $\begin{pmatrix} x_1 \\ x_2 \end{pmatrix}$

A_2 = state coefficient matrix = $\begin{pmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{pmatrix}$

$\mathbf{u}_1$ = source vector = 0

B_2 = source coefficient matrix = $\begin{pmatrix} 0 \\ 0 \end{pmatrix}$

In feedback systems, the duty cycle k is a function of $\mathbf{x}$ and may be a function of $\mathbf{u}$ as well. Thus, the total solution can be obtained by state–space averaging, that is, by summing the terms for each analysis the switched linear mode. Using the universal

format, we get

$$A = A_1 k + A_2(1 - k) \tag{5.139}$$

$$B = B_1 k + B_2(1 - k) \tag{5.140}$$

Substituting for A_1, A_2, B_1, and B_2, we can find

$$A = \begin{pmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{1}{RC} \end{pmatrix} \tag{5.141}$$

$$B = \begin{pmatrix} \frac{k}{L} \\ 0 \end{pmatrix} \tag{5.142}$$

which in turn lead to the following state equations:

$$x_1' = \frac{-1}{L} x_2 + \frac{k}{L} u_1 \tag{5.143}$$

$$x_2' = \frac{-1}{C} x_2 + \frac{1}{RC} x_2 \tag{5.144}$$

A continuous but nonlinear circuit that is described by Eqs. (5.143) and (5.144) is shown in Figure 5.33. It is a nonlinear circuit because k in general can be a function of x_1, x_2, and u_1.

The state–space averaging is an approximation technique that, for high enough switching frequencies, allows a continuous-time signal frequency analysis to be carried out separately from the switching frequency analysis. Although the original system is linear for any given switch condition, the resulting system (i.e., in Figure 5.33) generally is nonlinear. Therefore, small-signal approximations have to be employed to obtain the linearized small-signal behavior before other techniques [27, 28], such as Laplace transforms and Bode plots, can be applied.

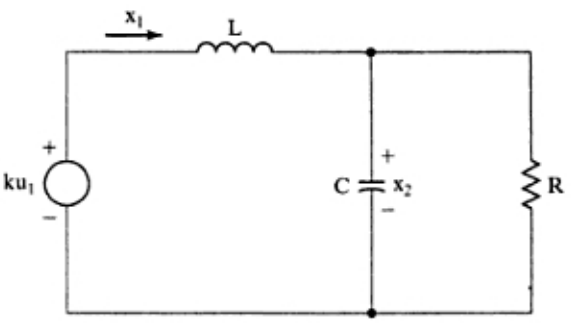


FIGURE 5.33

Continuous equivalent circuit of the Buck converter with state variables.

Key Points of Section 5.13

- The state–space averaging is an approximate technique that can be applied to describe the input and output relations of a switching converter, having different switching modes of operation. Although the original system is linear for any given switch condition, the resulting system generally is nonlinear. Therefore, small-signal approximations have to be employed to obtain the linearized small-signal behavior before other techniques can be applied.

SUMMARY

A dc converter can be used as a dc transformer to step up or step down a fixed dc voltage. The converter can also be used for switching-mode voltage regulators and for transferring energy between two dc sources. However, harmonics are generated at the input and load side of the converter, and these harmonics can be reduced by input and output filters. A converter can operate on either fixed frequency or variable frequency. A variable-frequency converter generates harmonics of variable frequencies and a filter design becomes difficult. A fixed-frequency converter is normally used. To reduce the sizes of filters and to lower the load ripple current, the chopping frequency should be high. The state–space averaging technique can be applied to describe the input and output relations of a switching converter, having different switching modes of operation.

REFERENCES

[1] J. A. M. Bleijs, and J. A. Gow, "Fast maximum power point control of current-fed DC–DC converter for photovoltaic arrays," *Electronics Letters*, Vol. 37, No. 1, January 2001, pp. 5–6.

[2] A. J. Forsyth, and S. V. Mollov, "Modeling and control of DC–DC converters," *Power Engineering Journal*, Vol. 12, No. 5, 1998, pp. 229–236.

[3] A. L. Baranovski, A. Mogel, W. Schwarz, and O. Woywode, "Chaotic control of a DC-DC-Converter," *Proc. IEEE International Symposium on Circuits and Systems*, Geneva, Switzerland, 2000, Vol. 2, pp. II-108–II-111.

[4] H. Matsuo, F. Kurokawa, H. Etou, Y. Ishizuka, and C. Chen, Changfeng, "Design oriented analysis of the digitally controlled dc–dc converter," *Proc. IEEE Power Electronics Specialists Conference*, Galway, U.K., 2000, pp. 401–407.

[5] J. L. Rodriguez Marrero, R. Santos Bueno, and G. C. Verghese, "Analysis and control of chaotic DC–DC switching power converters," *Proc. IEEE International Symposium on Circuits and Systems*, Orlando, FL, Vol. 5, 1999, pp. V-287–V-292.

[6] G. Ioannidis, A. Kandianis, and S. N. Manias, "Novel control design for the buck converter," *IEE Proceedings: Electric Power Applications*, Vol. 145, No. 1, January 1998, pp. 39–47.

[7] R. Oruganti, and M. Palaniapan, "Inductor voltage control of buck-type single-phase ac–dc converter," *IEEE Transactions on Power Electronics*, Vol. 15, No. 2, 2000, pp. 411–417.

[8] V. J. Thottuvelil, and G. C. Verghese, "Analysis and control design of paralleled DC/DC converters with current sharing," *IEEE Transactions on Power Electronics*, Vol. 13, No. 4, 1998, pp. 635–644.

[9] Y. Berkovich, and A. Ioinovici, "Dynamic model of PWM zero-voltage-transition DC–DC boost converter," *Proc. IEEE International Symposium on Circuits and Systems*, Orlando, FL, Vol. 5, 1999, pp. V-254–V-25.

[10] S. Cúk and R. D. Middlebrook, "Advances in switched mode power conversion," *IEEE Transactions on Industrial Electronics*, Vol. IE30, No. 1, 1983, pp. 10–29.

[11] K. Kit Sum, *Switch Mode Power Conversion—Basic Theory and Design*. New York: Marcel Dekker. 1984, Chapter 1.

[12] D. Ma, W. H. Ki, C. Y. Tsui, and P. K. T. Mok, "A 1.8-V single-inductor dual-output switching converter for power reduction techniques," Symposium on VLSI Circuits, 2001, pp. 137–140.

[13] R. D. Middlebrook and S. Cúk, "A general unified approach to modeling dc-to-dc converters in discontinuous conduction mode," *IEEE Power Electronics Specialist Conference*, 1977, pp. 36–57.

[14] H. S. H. Chung, "Design and analysis of a switched-capacitor-based step-up DC/DC converter with continuous input current," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 46, No. 6, 1999, pp. 722–730.

[15] H. S. H. Chung, S. Y. R. Hui, and S. C. Tang, "Development of low-profile DC/DC converter using switched-capacitor circuits and coreless PCB gate drive," *Proc. IEEE Power Electronics Specialists Conference*, Charleston, SC, Vol. 1, 1999, pp. 48–53.

[16] M. Kazerani, P. D. Ziogas, and G. Ioos, "A novel active current wave shaping technique for solid-state input power factor conditioners," *IEEE Transactions on Industrial Electronics*, Vol. IE38, No. 1, 1991, pp. 72–78.

[17] B. I. Takahashi, "Power factor improvements of a diode rectifier circuit by dither signals," *Conference Proc. IEEE-IAS Annual Meeting*, Seattle, WA, October 1990, pp. 1279–1294.

[18] A. R. Prasad and P. D. Ziogas, "An active power factor correction technique for three phase diode rectifiers," *IEEE Transactions on Power Electronics*, Vol. 6, No. 1, 1991, pp. 83–92.

[19] A. R. Prasad, P. D. Ziogas, and S. Manias, "A passive current wave shaping method for three phase diode rectifiers," *Proc. IEEE APEC-91 Conference Record*, 1991, pp. 319–330.

[20] M. S. Dawande, and G. K. Dubey, "Programmable input power factor correction method for switch-mode rectifiers," *IEEE Transactions on Power Electronics*, Vol. 2, No. 4, 1996, pp. 585–591.

[21] M. S. Dawande, V. R. Kanetkar, and G. K. Dubey, "Three-phase switch mode rectifier with hysteresis current control," *IEEE Transactions on Power Electronics*, Vol. 2, No. 3, 1996, pp. 466–471.

[22] E. L. M. Mehl, and I. Barbi, "An improved high-power factor and low-cost three-phase rectifier," *IEEE Transactions on Industry Applications*, Vol. 33, No. 2, 1997, pp. 485–492.

[23] F. Daniel, R. Chaffai, and K. Al-Haddad, "Three-phase diode rectifier with low harmonic distortion to feed capacitive loads," *IEEE APEC Conference Proc.*, 1996, pp. 932–938.

[24] M. Florez-Lizarraga and A. F. Witulski, Input filter design for multiple-module DC power systems," *IEEE Transactions on Power Electronics*, Vol. 2, No. 3, 1996, pp. 472–479.

[25] M. Alfayyoumi, A. H. Nayfeh, and D. Borojevic, "Input filter interactions in DC–DC switching regulators," *Proc. IEEE Power Electronics Specialists Conference*, Charleston, SC, Vol. 2, 1999, pp. 926–932.

[26] D. M. Mitchell, *DC–DC Switching Regulator*. New York: McGraw-Hill. 1988, Chapters 2 and 4.

[27] B. Lehman and R. M. Bass, "Extensions of averaging theory for power electronic systems," *IEEE Transactions on Power Electronics*, Vol. 2, No. 4, 1996, pp. 542–553.

[28] H. Bevrani, M. Abrishamchian, and N. Safari-shad," Nonlinear and linear robust control of switching power converters," *Proc. IEEE International Conference on Control Applications*, Vol. 1, 1999, pp. 808–813.

[29] C. A. Mufioz, and I. Barbi, "A new high-power-factor three-phase ac–dc converter: analysis, design, and experimentation," *IEEE Transactions on Power Electronics*, Vol. 14, No. 1, January 1999, pp. 90–97.

[30] *IEC Publication 555:* Disturbances in supply systems caused by household appliances and similar equipment; Part 2: Harmonics.

[31] Y. Jang, and M. M. Jovanovic, "A new input-voltage feed forward harmonic-injection technique with nonlinear gain control for single-switch, three-phase, DCM boost rectifiers." *IEEE Transactions on Power Electronics*, Vol. 28, No. 1, March 2000, pp. 268–277.

[32] M. H. Rashid, *SPICE for Power Electronics Using PSpice*. Englewood Cliffs, N.J.: Prentice-Hall. 1993, Chapters 10 and 11.

[33] P. Wood, *Switching Power Converters*. New York: Van Nostrand Reinhold. 1981.

[34] R. P. Severns and G. E. Bloom, *Modern DC-to-DC Switch Mode Power Converter Circuits*. New York: Van Nostrand Reinhold. 1983.

REVIEW QUESTIONS

5.1 What is a dc chopper, or dc–dc converter?
5.2 What is the principle of operation of a step-down converter?
5.3 What is the principle of operation of a step-up converter?
5.4 What is pulse-width-modulation control of a converter?
5.5 What is frequency-modulation control of a converter?
5.6 What are the advantages and disadvantages of a variable-frequency converter?
5.7 What is the effect of load inductance on the load ripple current?
5.8 What is the effect of chopping frequency on the load ripple current?
5.9 What are the constraints for controllable transfer of energy between two dc voltage sources?
5.10 What is the algorithm for generating the duty cycle of a converter?
5.11 What is the modulation index for a PWM control?
5.12 What is a first and second quadrant converter?
5.13 What is a third and fourth quadrant converter?
5.14 What is a four-quadrant converter?
5.15 What are the performance parameters of a converter?
5.16 What is a switching-mode regulator?
5.17 What are the four basic types of switching-mode regulators?
5.18 What are the advantages and disadvantages of a buck regulator?
5.19 What are the advantages and disadvantages of a boost regulator?
5.20 What are the advantages and disadvantages of a buck–boost regulator?
5.21 What are the advantages and disadvantages of a Cúk regulator?
5.22 At what duty cycle does the load ripple current become maximum?
5.23 What are the effects of chopping frequency on filter sizes?
5.24 What is the discontinuous mode of operation of a regulator?
5.25 What is a multioutput boost converter?
5.26 Why must the multioutput boost converter be operated with time multiplexing control?
5.27 Why must the multioutput boost converter be operated in discontinuous mode?
5.28 How can the input current of the rectifier-fed boost converter be made sinusoidal and in phase with the input voltage?
5.29 What is a state–space averaging technique?

PROBLEMS

5.1 The dc converter in Figure 5.1a has a resistive load, $R = 20\ \Omega$ and input voltage, $V_s = 220$ V. When the converter remains on, its voltage drop is $V_{ch} = 1.5$ V and chopping frequency is $f = 10$ kHz. If the duty cycle is 80%, determine **(a)** the average output voltage V_a, **(b)** the rms output voltage V_o, **(c)** the converter efficiency, **(d)** the effective input resistance R_i, and **(e)** the rms value of the fundamental component of harmonics on the output voltage.

5.2 A converter is feeding an RL load as shown in Figure 5.3 with $V_s = 220$ V, $R = 10\ \Omega$, $L = 15.5$ mH, $f = 5$ kHz, and $E = 20$ V. Calculate **(a)** the minimum instantaneous load current I_1, **(b)** the peak instantaneous load current I_2, **(c)** the maximum peak-to-peak ripple current in the load, **(d)** the average load current I_a, **(e)** the rms load current I_o, **(f)** the effective input resistance R_i, and **(g)** the rms value of converter current I_R.

5.3 The converter in Figure 5.3 has load resistance, $R = 0.2\ \Omega$; input voltage $V_s = 220$ V; and battery voltage, $E = 10$ V. The average load current, $I_a = 200$ A, and the chopping frequency is $f = 200$ Hz ($T = 5$ ms). Use the average output voltage to calculate the value of load inductance L, which would limit the maximum load ripple current to 5% of I_a.

5.4 The dc converter shown in Figure 5.7a is used to control power flow from a dc voltage, $V_s = 110$ V to a battery voltage, $E = 220$ V. The power transferred to the battery is 30 kW. The current ripple of the inductor is negligible. Determine **(a)** the duty cycle K, **(b)** the effective load resistance R_{eq}, and **(c)** the average input current I_s.

5.5 For Problem 5.4, plot the instantaneous inductor current and current through the battery E if inductor L has a finite value of $L = 7.5$ mH, $f = 250$ Hz, and $k = 0.5$.

5.6 An RL load as shown in Figure 5.3 is controlled by a converter. If load resistance $R = 0.25\ \Omega$, inductance $L = 20$ mH, supply voltage $V_s = 600$, battery voltage $E = 150$ V, and chopping frequency $f = 250$ Hz, determine the minimum and maximum load current, the peak-to-peak load ripple current, and average load current for $k = 0.1$ to 0.9 with a step of 0.1.

5.7 Determine the maximum peak-to-peak ripple current of Problem 5.6 by using Eqs. (5.21) and (5.22), and compare the results.

5.8 The step-up converter in Figure 5.8a has $R = 10\ \Omega$, $L = 6.5$ mH, $E = 5$ V, and $k = 0.5$. Find I_1, I_2, and ΔI. Use SPICE to find these values and plot the load, diode, and switch current.

5.9 The buck regulator in Figure 5.16a has an input voltage, $V_s = 15$ V. The required average output voltage $V_a = 5$ V and the peak-to-peak output ripple voltage is 10 mV. The switching frequency is 20 kHz. The peak-to-peak ripple current of inductor is limited to 0.5 A. Determine **(a)** the duty cycle k, **(b)** the filter inductance L, **(c)** the filter capacitor C, and **(d)** the critical values of L and C.

5.10 The boost regulator in Figure 5.17a has an input voltage, $V_s = 6$ V. The average output voltage, $V_a = 15$ V and average load current, $I_a = 0.5$ A. The switching frequency is 20 kHz. If $L = 250\ \mu$H and $C = 440\ \mu$F, determine **(a)** the duty cycle k **(b)** the ripple current of inductor, ΔI, **(c)** the peak current of inductor, I_2, **(d)** the ripple voltage of filter capacitor, ΔV_c, and **(e)** the critical values of L and C.

5.11 The buck–boost regulator in Figure 5.18a has an input voltage, $V_s = 12$ V. The duty cycle, $k = 0.6$, and the switching frequency is 25 kHz. For the inductance, $L = 250\ \mu$H and for filter capacitance, $C = 220\ \mu$F. For the average load current, $I_a = 1.5$ A. Determine **(a)** the average output voltage V_a, **(b)** the peak-to-peak output ripple voltage ΔV_c, **(c)** the peak-to-peak ripple current of inductor ΔI, **(d)** the peak current of the transistor I_p, and **(e)** the critical values of L and C.

5.12 The Cúk regulator in Figure 5.19a has an input voltage, $V_s = 15$ V. The duty cycle is $k = 0.4$ and the switching frequency is 25 kHz. The filter inductance is $L_2 = 350\ \mu$H and

filter capacitance is $C_2 = 220\ \mu F$. The energy transfer capacitance is $C_1 = 400\ \mu F$ and inductance is $L_1 = 250\ \mu H$. The average load current is $I_a = 1.25$ A. Determine **(a)** the average output voltage V_a, **(b)** the average input current I_s, **(c)** the peak-to-peak ripple current of inductor L_1, ΔI_1, **(d)** the peak-to-peak ripple voltage of capacitor C_1, ΔV_{c1}, **(e)** the peak-to-peak ripple current of inductor L_2, ΔI_2, **(f)** the peak-to-peak ripple voltage of capacitor C_2, ΔV_{c2}, and **(g)** the peak current of the transistor I_p.

5.13 In Problem 5.12 for the Cúk regulator, find the critical values of L_1, C_1, L_2, and C_2.

5.14 The buck converter in Figure 5.29 has a dc input voltage $V_s = 110$ V, average load voltage $V_a = 80$ V, and average load current $I_a = 20$ A. The chopping frequency is $f = 10$ kHz. The peak-to-peak ripples are 5% for load voltage, 2.5% for load current, and 10% for filter L_e current. **(a)** Determine the values of L_e, L, and C_e. Use PSpice **(b)** to verify the results by plotting the instantaneous capacitor voltage v_C and instantaneous load current i_L, and **(c)** to calculate the Fourier coefficients of the input current i_s. Use SPICE model parameters of Example 5.10.

5.15 The boost converter in Figure 5.17a has a dc input voltage $V_S = 5$ V. The load resistance R is 100 Ω. The inductance is $L = 150\ \mu H$, and the filter capacitance is $C = 220\ \mu F$. The chopping frequency is $f = 20$ kHz and the duty cycle of the converter is $k = 60\%$. Use PSpice **(a)** to plot the output voltage v_C, the input current i_s, and the MOSFET voltage v_T; and **(b)** to calculate the Fourier coefficients of the input current i_s. The SPICE model parameters of the MOSFET are L = 2U, W = 0.3, VTO = 2.831, KP = 20.53U, IS = 194E−18, CGSO = 9.027N, CGDO = 1.679N.

5.16 A dc regulator is operated at a duty cycle of $k = 0.4$. The load resistance is $R = 150\ \Omega$, the inductor resistance is $r_L = 1\ \Omega$, and the resistance of the filter capacitor is $r_c = 0.2\ \Omega$. Determine the voltage gain for the **(a)** buck converter, **(b)** boost converter and **(c)** buck–boost converter.

CHAPTER 6

Pulse-Width-Modulated Inverters

The learning objectives of this chapter are as follows:

- To learn the switching technique for dc–ac converters known as inverters and the types of inverters
- To study the operation of inverters
- To understand the performance parameters of inverters
- To learn the different types of modulation techniques to obtain a near sinusoidal output waveform and the techniques to eliminate certain harmonics from the output
- To learn the techniques for analyzing and designing inverters and for simulating inverters by using SPICE
- To study the effects of load impedance on the load current

6.1 INTRODUCTION

Dc-to-ac converters are known as *inverters*. The function of an inverter is to change a dc input voltage to a symmetric ac output voltage of desired magnitude and frequency [1]. The output voltage could be fixed or variable at a fixed or variable frequency. A variable output voltage can be obtained by varying the input dc voltage and maintaining the gain of the inverter constant. On the other hand, if the dc input voltage is fixed and it is not controllable, a variable output voltage can be obtained by varying the gain of the inverter, which is normally accomplished by pulse-width-modulation (PWM) control within the inverter. The *inverter gain* may be defined as the ratio of the ac output voltage to dc input voltage.

The output voltage waveforms of ideal inverters should be sinusoidal. However, the waveforms of practical inverters are nonsinusoidal and contain certain harmonics. For low- and medium-power applications, square-wave or quasi-square-wave voltages may be acceptable; and for high-power applications, low distorted sinusoidal waveforms are required. With the availability of high-speed power semiconductor devices,

the harmonic contents of output voltage can be minimized or reduced significantly by switching techniques.

Inverters are widely used in industrial applications (e.g., variable-speed ac motor drives, induction heating, standby power supplies, and uninterruptible power supplies). The input may be a battery, fuel cell, solar cell, or other dc source. The typical single-phase outputs are (1) 120 V at 60 Hz, (2) 220 V at 50 Hz, and (3) 115 V at 400 Hz. For high-power three-phase systems, typical outputs are (1) 220 to 380 V at 50 Hz, (2) 120 to 208 V at 60 Hz, and (3) 115 to 200 V at 400 Hz.

Inverters can be broadly classified into two types: (1) single-phase inverters, and (2) three-phase inverters. Each type can use controlled turn-on and turn-off devices (e.g., bipolar junction transistors [BJTs], metal oxide semiconductor field-effect transistors [MOSFETs], insulated-gate bipolar transistors [IGBTs], metal oxide semiconductor-controlled thyristors [MCTs], static induction transistors, [SITs], and gate-turn-off thyristors [GTOs]). These inverters generally use PWM control signals for producing an ac output voltage. An inverter is called a *voltage-fed inverter* (VFI) if the input voltage remains constant, a *current-fed inverter* (CFI) if the input current is maintained constant, and a *variable dc linked inverter* if the input voltage is controllable. If the output voltage or current of the inverter is forced to pass through zero by creating an LC resonant circuit, this type of inverter is called *resonant-pulse inverter* and it has wide applications in power electronics. Chapter 8 is devoted to resonant-pulse inverters only.

6.2 PRINCIPLE OF OPERATION

The principle of single-phase inverters [1] can be explained with Figure 6.1a. The inverter circuit consists of two choppers. When only transistor Q_1 is turned on for a time $T_0/2$, the instantaneous voltage across the load v_0 is $V_s/2$. If transistor Q_2 only is turned on for a time $T_0/2$, $-V_s/2$ appears across the load. The logic circuit should be designed such that Q_1 and Q_2 are not turned on at the same time. Figure 6.1b shows the waveforms for the output voltage and transistor currents with a resistive load. This inverter requires a three-wire dc source, and when a transistor is off, its reverse voltage is V_s instead of $V_s/2$. This inverter is known as a *half-bridge inverter*.

The root-mean-square (rms) output voltage can be found from

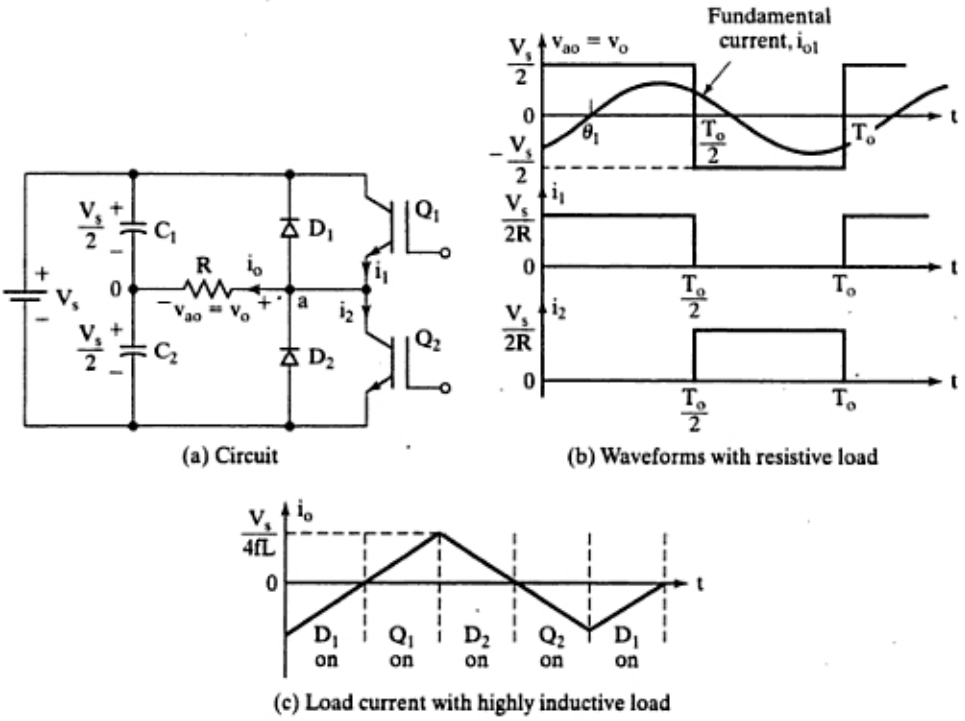
$$V_o = \left(\frac{2}{T_0}\int_0^{T_0/2}\frac{V_s^2}{4}\,dt\right)^{1/2} = \frac{V_s}{2} \tag{6.1}$$

The instantaneous output voltage can be expressed in Fourier series as

$$v_o = \frac{a_0}{2} + \sum_{n=1}^{\infty}\left(a_n\cos(n\omega t) + b_n\sin(n\omega t)\right)$$

Due to the quarter-wave symmetry along the x-axis, both a_0 and a_n are zero. We get b_n as

$$b_n = \frac{1}{\pi}\left[\int_{-\frac{\pi}{2}}^{0}\frac{-V_s}{2}\,d(\omega t) + \int_0^{\frac{\pi}{2}}\frac{V_s}{2}\,d(\omega t)\right] = \frac{4V_s}{n\pi}$$



(a) Circuit

(b) Waveforms with resistive load

(c) Load current with highly inductive load

FIGURE 6.1
Single-phase half-bridge inverter.

which gives the instantaneous output voltage v_o as

$$v_0 = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2V_s}{n\pi} \sin n\omega t$$
$$= 0 \qquad \text{for } n = 2, 4, \ldots \tag{6.2}$$

where $\omega = 2\pi f_0$ is the frequency of output voltage in rads per second. Due to the quarter-wave symmetry of the output voltage along the x-axis, the even harmonics voltages are absent. For $n = 1$, Eq. (6.2) gives the rms value of fundamental component as

$$V_{o1} = \frac{2V_s}{\sqrt{2}\pi} = 0.45V_s \tag{6.3}$$

For an inductive load, the load current cannot change immediately with the output voltage. If Q_1 is turned off at $t = T_0/2$, the load current would continue to flow through D_2, load, and lower half of the dc source until the current falls to zero. Similary, when Q_2 is turned off at $t = T_0$, the load current flows through D_1, load, and upper half of the dc source. When diode D_1 or D_2 conducts, energy is fed back to the dc source and these diodes are known as *feedback diodes*. Figure 6.1c shows the load current and conduction intervals of devices for a purely inductive load. It can be noticed that for a purely

inductive load, a transistor conducts only for $T_0/2$ (or 90°). Depending on the load impedance angle, the conduction period of a transistor would vary from 90° to 180°.

Any switching devices can replace the transistors. If t_{off} is the turn-off time of a device, there must be a minimum delay time of $t_d (= t_{off})$ between the outgoing device and triggering of the next incoming device. Otherwise, short-circuit condition would result through the two devices. Therefore, the maximum conduction time of a device would be $t_{on} = T_o/2 - t_d$. All practical devices require a certain turn-on and turn-off time. For successful operation of inverters, the logic circuit should take these into account.

For an RL load, the instantaneous load current i_0 can be found by dividing the instantaneous output voltage by the load impedance $Z = R + jn\omega L$. Thus, we get

$$i_0 = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2V_s}{n\pi\sqrt{R^2 + (n\omega L)^2}} \sin(n\omega t - \theta_n) \tag{6.4}$$

where $\theta_n = \tan^{-1}(n\omega L/R)$. If I_{01} is the rms fundamental load current, the fundamental output power (for $n = 1$) is

$$P_{01} = V_{o1} I_{01} \cos\theta_1 = I_{01}^2 R \tag{6.5}$$

$$= \left[\frac{2V_s}{\sqrt{2}\pi\sqrt{R^2 + (\omega L)^2}}\right]^2 R \tag{6.5a}$$

Note: In most applications (e.g., electric motor drives) the output power due to the fundamental current is generally the useful power, and the power due to harmonic currents is dissipated as heat and increases the load temperature.

Dc supply current. Assuming a lossless inverter, the average power absorbed by the load must be equal to the average power supplied by the dc source. Thus, we can write

$$\int_0^T v_s(t) i_s(t) dt = \int_0^T v_o(t) i_o(t) dt$$

where T is the period of the ac output voltage. For an inductive load and a relatively high switching frequency, the load current i_o is nearly sinusoidal; therefore, only the fundamental component of the ac output voltage provides power to the load. Because the dc supply voltage remains constant $v_s(t) = V_s$, we can write

$$\int_0^T i_s(t) dt = \frac{1}{V_s} \int_0^T \sqrt{2} V_{o1} \sin(\omega t) \sqrt{2} I_o \sin(\omega t - \theta_1) dt = I_s$$

where V_{o1} is the fundamental rms output voltage;
I_o is the rms load current;
θ_1 is the load angle at the fundamental frequency.

Thus, the dc supply current I_s can be simplified to

$$I_s = \frac{V_{o1}}{V_s} I_o \cos(\theta_1) \tag{6.6}$$

Gating sequence. The gating sequence for the switching devices is as follows:

1. Generate a square-wave gating-signal v_{g1} at an output frequency f_o and a 50% duty cycle. The gating-signal v_{g2} should be a logic invert of v_{g1}.
2. Signal v_{g1} will drive switch Q_1 through a gate-isolating circuit, and v_{g2} can drive Q_2 without any isolating circuit.

Key Points of Section 6.2

- An ac output voltage can be obtained by alternatively connecting the positive and negative terminals of the dc source across the load by turning on and off the switching devices accordingly. The rms fundamental component V_{o1} of the output voltage is 0.45 V_s.
- Feedback diodes are required to transfer the energy stored in the load inductance back to the dc source.

6.3 PERFORMANCE PARAMETERS

The output of practical inverters contain harmonics and the quality of an inverter is normally evaluated in terms of the following performance parameters.

Harmonic factor of *n*th harmonic (HF_n). The harmonic factor (of the *n*th harmonic), which is a measure of individual harmonic contribution, is defined as

$$HF_n = \frac{V_{on}}{V_{o1}} \qquad \text{for } n > 1 \tag{6.7}$$

where V_1 is the rms value of the fundamental component and V_{on} is the rms value of the *n*th harmonic component.

Total harmonic distortion (THD). The total harmonic distortion, which is a measure of closeness in shape between a waveform and its fundamental component, is defined as

$$\text{THD} = \frac{1}{V_{o1}} \left(\sum_{n=2,3,\ldots}^{\infty} V_{on}^2 \right)^{1/2} \tag{6.8}$$

Distortion factor (DF). THD gives the total harmonic content, but it does not indicate the level of each harmonic component. If a filter is used at the output of inverters, the higher order harmonics would be attenuated more effectively. Therefore, a knowledge of both the frequency and magnitude of each harmonic is important. The DF indicates the amount of HD that remains in a particular waveform after the harmonics of that waveform have been subjected to a second-order attenuation (i.e.,

divided by n^2). Thus, DF is a measure of effectiveness in reducing unwanted harmonics without having to specify the values of a second-order load filter and is defined as

$$\mathrm{DF} = \frac{1}{V_{o1}}\left[\sum_{n=2,3,\ldots}^{\infty}\left(\frac{V_{on}}{n^2}\right)^2\right]^{1/2} \tag{6.9}$$

The DF of an individual (or nth) harmonic component is defined as

$$\mathrm{DF}_n = \frac{V_{on}}{V_{o1}n^2} \qquad \text{for } n > 1 \tag{6.10}$$

Lowest order harmonic (LOH). The LOH is that harmonic component whose frequency is closest to the fundamental one, and its amplitude is greater than or equal to 3% of the fundamental component.

Example 6.1 Finding the Parameters of the Single-Phase Half-Bridge Inverter

The single-phase half-bridge inverter in Figure 6.1a has a resistive load of $R = 2.4\ \Omega$ and the dc input voltage is $V_s = 48$ V. Determine (a) the rms output voltage at the fundamental frequency V_{o1}, (b) the output power P_o, (c) the average and peak currents of each transistor, (d) the peak reverse blocking voltage V_{BR} of each transistor, (e) the THD, (f) the DF, and (g) the HF and DF of the LOH.

Solution

$V_s = 48$ V and $R = 2.4\ \Omega$.

a. From Eq. (6.3), $V_{o1} = 0.45 \times 48 = 21.6$ V.

b. From Eq. (6.1), $V_o = V_s/2 = 48/2 = 24$ V. The output power, $P_o = V_o^2/R = 24^2/2.4 = 240$ W.

c. The peak transistor current $I_p = 24/2.4 = 10$ A. Because each transistor conducts for a 50% duty cycle, the average current of each transistor is $I_Q = 0.5 \times 10 = 5$ A.

d. The peak reverse blocking voltage $V_{BR} = 2 \times 24 = 48$ V.

e. From Eq. (6.3), $V_{o1} = 0.45V_s$ and the rms harmonic voltage V_h

$$V_h = \left(\sum_{n=3,5,7,\ldots}^{\infty} V_{on}^2\right)^{1/2} = (V_0^2 - V_{o1}^2)^{1/2} = 0.2176V_s$$

From Eq. (6.8), $\mathrm{THD} = (0.2176V_s)/(0.45V_s) = 48.34\%$.

f. From Eq. (6.2), we can find V_{on} and then find,

$$\left[\sum_{n=3,5,\ldots}^{\infty}\left(\frac{V_{on}}{n^2}\right)^2\right]^{1/2} = \left[\left(\frac{V_{o3}}{3^2}\right)^2 + \left(\frac{V_{o5}}{5^2}\right)^2 + \left(\frac{V_{o7}}{7^2}\right)^2 + \cdots\right]^{1/2} = 0.024V_s$$

From Eq. (6.9), $\mathrm{DF} = 0.024V_s/(0.45V_s) = 5.382\%$.

g. The LOH is the third, $V_{o3} = V_{o1}/3$. From Eq. (6.7), $\mathrm{HF}_3 = V_{o3}/V_{o1} = 1/3 = 33.33\%$, and from Eq. (6.10), $\mathrm{DF}_3 = (V_{o3}/3^2)/V_{o1} = 1/27 = 3.704\%$. Because $V_{o3}/V_{o1} = 33.33\%$, which is greater than 3%, $\mathrm{LOH} = V_{o3}$.

Key Points of Section 6.3

- The performance parameters, which measure the quality of the inverter output voltage, are HF, THD, DF, and LOH.

6.4 SINGLE-PHASE BRIDGE INVERTERS

A single-phase bridge voltage source inverter (VSI) is shown in Figure 6.2a. It consists of four choppers. When transistors Q_1 and Q_2 are turned on simultaneously, the input voltage V_s appears across the load. If transistors Q_3 and Q_4 are turned on at the same time, the voltage across the load is reversed and is $-V_s$. The waveform for the output voltage is shown in Figure 6.2b.

Table 6.1 shows the five switch states. Transistors Q_1, Q_4 in Figure 6.2a act as the switching devices S_1, S_4, respectively. If two switches: one upper and one lower conduct at the same time such that the output voltage is $\pm V_s$, the switch state is 1, whereas if these switches are off at the same time, the switch state is 0.

The rms output voltage can be found from

$$V_o = \left(\frac{2}{T_0}\int_0^{T_0/2} V_s^2\, dt\right)^{1/2} = V_s \tag{6.11}$$

Equation (6.2) can be extended to express the instantaneous output voltage in a Fourier series as

$$v_o = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_s}{n\pi} \sin n\omega t \tag{6.12}$$

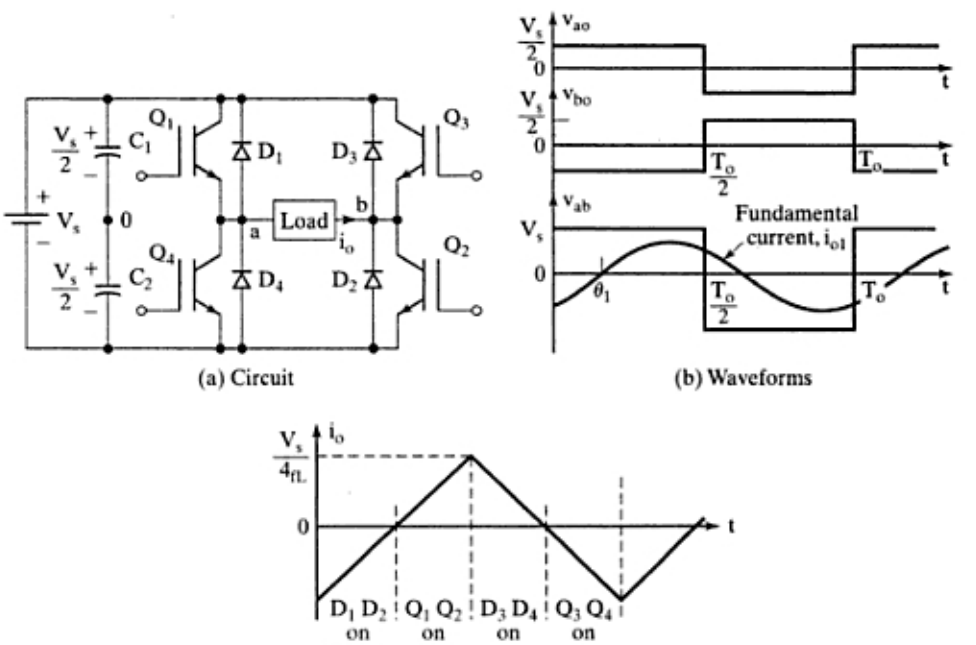


FIGURE 6.2

Single-phase full-bridge inverter.

TABLE 6.1 Switch States for a Single-Phase Full-Bridge Voltage-Source Inverter (VSI)

State	State No.	Switch State*	v_{ao}	v_{bo}	v_o	Components Conducting
S_1 and S_2 are on and S_4 and S_3 are off	1	10	$V_S/2$	$-V_S/2$	V_S	S_1 and S_2 if $i_o > 0$ D_1 and D_2 if $i_o < 0$
S_4 and S_3 are on and S_1 and S_2 are off	2	01	$-V_S/2$	$V_S/2$	$-V_S$	D_4 and D_3 if $i_o > 0$ S_4 and S_3 if $i_o < 0$
S_1 and S_3 are on and S_4 and S_2 are off	3	11	$V_S/2$	$V_S/2$	0	S_1 and D_3 if $i_o > 0$ D_1 and S_3 if $i_o < 0$
S_4 and S_2 are on and S_1 and S_3 are off	4	00	$-V_S/2$	$-V_S/2$	0	D_4 and S_2 if $i_o > 0$ S_4 and D_2 if $i_o < 0$
S_1, S_2, S_3, and S_4 are all off	5	off	$-V_S/2$ $V_S/2$	$V_S/2$ $-V_S/2$	$-V_S$ V_S	D_4 and D_3 if $i_o > 0$ D_4 and D_2 if $i_o < 0$

* 1 if an upper switch is on and 0 if a lower switch is on.

and for $n = 1$, Eq. (6.12) gives the rms value of fundamental component as

$$V_1 = \frac{4V_s}{\sqrt{2}\pi} = 0.90V_s \tag{6.13}$$

Using Eq. (6.4), the instantaneous load current i_0 for an RL load becomes

$$i_0 = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_s}{n\pi\sqrt{R^2 + (n\omega L)^2}} \sin(n\omega t - \theta_n) \tag{6.14}$$

where $\theta_n = \tan^{-1}(n\omega L/R)$.

When diodes D_1 and D_2 conduct, the energy is fed back to the dc source; thus, they are known as *feedback diodes*. Figure 6.2c shows the waveform of load current for an inductive load.

Dc supply current. Neglecting any losses, the instantaneous power balance gives,

$$v_s(t)i_s(t) = v_o(t)i_o(t)$$

For inductive load and relatively high-switching frequencies, the load current i_o and the output voltage may be assumed sinusoidal. Because the dc supply voltage remains constant $v_s(t) = V_s$, we get

$$i_s(t) = \frac{1}{V_s}\sqrt{2}V_{o1}\sin(\omega t)\sqrt{2}I_o\sin(\omega t - \theta_1)$$

which can be simplified to find the dc supply current as

$$i_s(t) = \frac{V_{o1}}{V_s}I_o\cos(\theta_1) - \frac{V_{o1}}{V_s}I_o\cos(2\omega t - \theta_1) \tag{6.15}$$

where V_{o1} is the fundamental rms output voltage;
I_o is the rms load current;
θ_1 is the load impedance angle at the fundamental frequency.

Equation (6.15) indicates the presence of a second-order harmonic of the same order of magnitude as the dc supply current. This harmonic is injected back into the dc

voltage source. Thus, the design should consider this to guarantee a nearly constant dc link voltage. A large capacitor is normally connected across the dc voltage source and such a capacitor is costly and demands space; both features are undesirable, especially in medium to high power supplies.

Example 6.2 Finding the Parameters of the Single-Phase Full-Bridge Inverter

Repeat Example 6.1 for a single-phase bridge inverter in Figure 6.2a.

Solution

$V_s = 48$ V and $R = 2.4\ \Omega$.

a. From Eq. (6.13), $V_1 = 0.90 \times 48 = 43.2$ V.

b. From Eq. (6.11), $V_o = V_s = 48$ V. The output power is $P_o = V_s^2/R = 48^2/2.4 = 960$ W.

c. The peak transistor current is $I_p = 48/2.4 = 20$ A. Because each transistor conducts for a 50% duty cycle, the average current of each transistor is $I_Q = 0.5 \times 20 = 10$ A.

d. The peak reverse blocking voltage is $V_{BR} = 48$ V.

e. From Eq. (6.13), $V_1 = 0.9V_s$. The rms harmonic voltage V_h is

$$V_h = \left(\sum_{n=3,5,7,\ldots}^{\infty} V_{on}^2\right)^{1/2} = (V_0^2 - V_{o1}^2)^{1/2} = 0.4352V_s$$

From Eq. (6.8), THD $= 0.4359V_s/(0.9V_s) = 48.34\%$.

f. $\left[\sum_{n=3,5,7,\ldots}^{\infty} \left(\frac{V_{on}}{n^2}\right)^2\right]^{1/2} = 0.048V_s$

From Eq. (6.9), DF $= 0.048V_s/(0.9V_s) = 5.382\%$.

g. The LOH is the third, $V_3 = V_1/3$. From Eq. (6.7), $HF_3 = V_{o3}/V_{o1} = 1/3 = 33.33\%$ and from Eq. (6.10), $DF_3 = (V_{o3}/3^2)/V_{o1} = 1/27 = 3.704\%$.

Note: The peak reverse blocking voltage of each transistor and the quality of output voltage for half-bridge and full-bridge inverters are the same. However, for full-bridge inverters, the output power is four times higher and the fundamental component is twice that of half-bridge inverters.

Example 6.3 Finding the Output Voltage and Current of a Single-Phase Full-Bridge Inverter with an *RLC* Load

The bridge inverter in Figure 6.2a has an *RLC* load with $R = 10\ \Omega$, $L = 31.5$ mH, and $C = 112\ \mu$F. The inverter frequency is $f_0 = 60$ Hz and dc input voltage is $V_s = 220$ V. (a) Express the instantaneous load current in Fourier series. Calculate (b) the rms load current at the fundamental frequency I_{o1}; (c) the THD of the load current; (d) the power absorbed by the load P_0 and the fundamental power P_{01}; (e) the average current of dc supply I_s; and (f) the rms and peak current of each transistor. (g) Draw the waveform of fundamental load current and show the conduction intervals of transistors and diodes. Calculate the conduction time of (h) the transistors, and (i) the diodes.

Solution

$V_s = 220$ V, $f_0 = 60$ Hz, $R = 10\ \Omega$, $L = 31.5$ mH, $C = 112\ \mu$F, and $\omega = 2\pi \times 60 = 377$ rad/s. The inductive reactance for the nth harmonic voltage is

$$X_L = j_n\omega L = j2n\pi \times 60 \times 31.5 \times 10^{-3} = j11.87n\ \Omega$$

The capacitive reactance for the nth harmonic voltage is

$$X_c = -\frac{j}{n\omega C} = -\frac{j10^6}{2n\pi \times 60 \times 112} = \frac{-j23.68}{n}\ \Omega$$

The impedance for the nth harmonic voltage is

$$|Z_n| = \sqrt{R^2 + \left(n\omega L - \frac{1}{n\omega C}\right)^2} = [10^2 + (11.87n - 23.68/n)^2]^{1/2}$$

and the load impedance angle for the nth harmonic voltage is

$$\theta_n = \tan^{-1}\frac{11.87n - 23.68/n}{10} = \tan^{-1}\left(1.187n - \frac{2.368}{n}\right)$$

a. From Eq. (6.12), the instantaneous output voltage can be expressed as

$$v_o(t) = 280.1\sin(377t) + 93.4\sin(3 \times 377t) + 56.02\sin(5 \times 377t) + 40.02\sin(7 \times 377t) + 31.12\sin(9 \times 377t) + \cdots$$

Dividing the output voltage by the load impedance and considering the appropriate delay due to the load impedance angles, we can obtain the instantaneous load current as

$$i_o(t) = 18.1\sin(377t + 49.72°) + 3.17\sin(3 \times 377t - 70.17°) + \sin(5 \times 377t - 79.63°) + 0.5\sin(7 \times 377t - 82.85°) + 0.3\sin(9 \times 377t - 84.52°) + \cdots$$

b. The peak fundamental load current is $I_{m1} = 18.1$ A. The rms load current at fundamental frequency is $I_{o1} = 18.1/\sqrt{2} = 12.8$ A.

c. Considering up to the ninth harmonic, the peak load current,

$$I_m = (18.1^2 + 3.17^2 + 1.0^2 + 0.5^2 + 0.3^2)^{1/2} = 18.41\ \text{A}$$

The rms harmonic load current is

$$I_h = (I_m^2 - I_{m1}^2)^{1/2} = \frac{18.41^2 - 18.1^2}{\sqrt{2}} = 2.3789\ \text{A}$$

Using Eq. (6.8), the THD of the load current,

$$\text{THD} = \frac{(I_m^2 - I_{m1}^2)^{1/2}}{I_{m1}} = \left[\left(\frac{18.41}{18.1}\right)^2 - 1\right]^{1/2} = .18.59\%$$

d. The rms load current is $I_o \cong I_m/\sqrt{2} = 18.41/\sqrt{2} = 13.02$ A, and the load power is $P_o = 13.02^2 \times 10 = 1695$ W. Using Eq. (6.5), the fundamental output power is

$$P_{o1} = I_{o1}^2 R = 12.8^2 \times 10 = 1638.4\ \text{W}$$

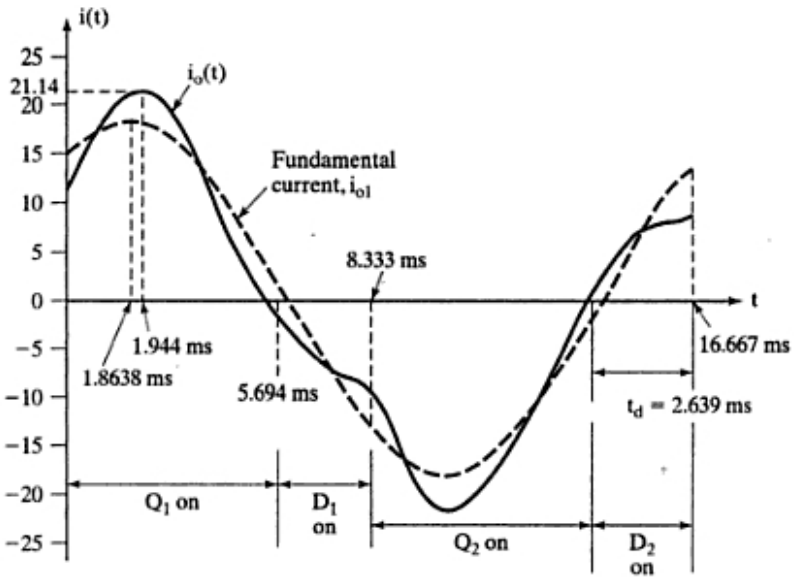


FIGURE 6.3

Waveforms for Example 6.3.

e. The average supply current $I_s = P_o/V_s = 1695/220 = 7.7$ A.

f. The peak transistor current $I_p \cong I_m = 18.41$ A. The maximum permissible rms current of each transistor is $I_{Q(\max)} = I_o/\sqrt{2} = I_p/2 = 18.41/2 = 9.2$ A.

g. The waveform for fundamental load current $i_1(t)$ is shown in Figure 6.3.

h. From Fig. (6.3), the conduction time of each transistor is found approximately from $\omega t_0 = 180 - 49.72 = 130.28°$ or $t_0 = 130.28 \times \pi/(180 \times 377) = 6031$ μs.

i. The conduction time of each diode is approximately

$$t_d = (180 - 130.28) \times \frac{\pi}{180 \times 377} = 2302 \text{ μs}$$

Notes:

1. To calculate the exact values of the peak current, the conduction time of transistors and diodes, the instantaneous load current $i_o(t)$ should be plotted as shown in Figure 6.3. The conduction time of a transistor must satisfy the condition $i_o(t = t_0) = 0$, and a plot of $i_o(t)$ by a computer program gives $I_p = 21.14$ A, $t_0 = 5694$ μs, and $t_d = 2639$ μs.
2. This example can be repeated to evaluate the performance of an inverter with R, RL, or RLC load with an appropriate change in load impedance Z_L and load angle θ_n.

Gating sequence. The gating sequence for the switching devices is as follows:

1. Generate two square-wave gating-signals v_{g1} and v_{g2} at an output frequency f_o and a 50% duty cycle. The gating-signals v_{g3} and v_{g4} should be the logic invert of v_{g2} and v_{g4}, respectively.

2. Signals v_{g1} and v_{g3} drive Q_1 and Q_3, respectively, through gate isolation circuits. Signals v_{g2} and v_{g4} can drive Q_2 and Q_4, respectively, without any isolation circuits.

Key Points of Section 6.4

- The full-bridge inverter requires four switching devices and four diodes. The output voltage switches between $+V_s$ and $-V_s$. The rms fundamental component V_1 of the output voltage is $0.9V_s$.
- The design of an inverter requires the determination of the average, rms, and peak currents of the switching devices and diodes.

6.5 THREE-PHASE INVERTERS

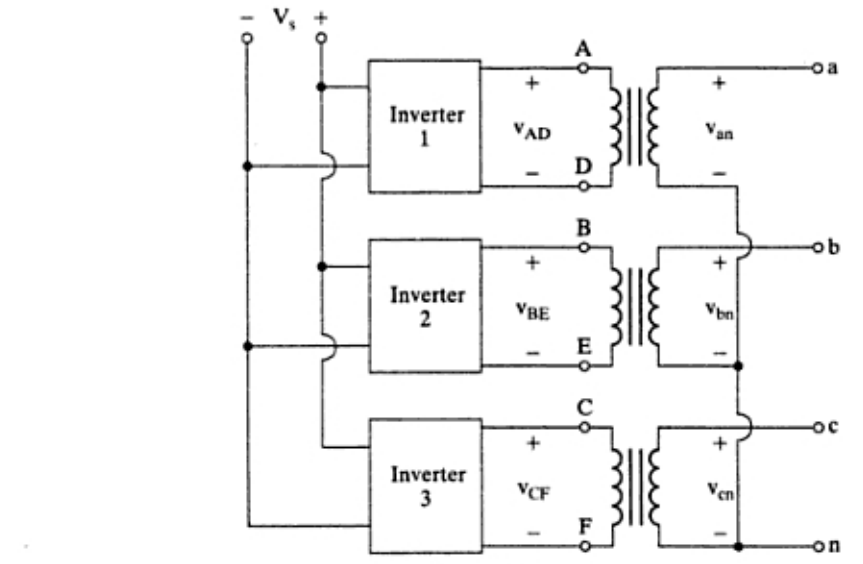
Three-phase inverters are normally used for high-power applications. Three single-phase half (or full)-bridge inverters can be connected in parallel as shown in Figure 6.4a to form the configuration of a three-phase inverter. The gating signals of single-phase inverters should be advanced or delayed by 120° with respect to each other to obtain three-phase balanced (fundamental) voltages. The transformer primary windings must be isolated from each other, whereas the secondary windings may be connected in Y or delta. The transformer secondary is normally connected in delta to eliminate triplen harmonics ($n = 3, 6, 9, \ldots$) appearing on the output voltages and the circuit arrangement is shown in Figure 6.4b. This arrangement requires three single-phase transformers, 12 transistors, and 12 diodes. If the output voltages of single-phase inverters are not perfectly balanced in magnitudes and phases, the three-phase output voltages are unbalanced.

A three-phase output can be obtained from a configuration of six transistors and six diodes as shown in Figure 6.5a. Two types of control signals can be applied to the transistors: 180° conduction or 120° conduction. The 180° conduction has better utilization of the switches and is the preferred method.

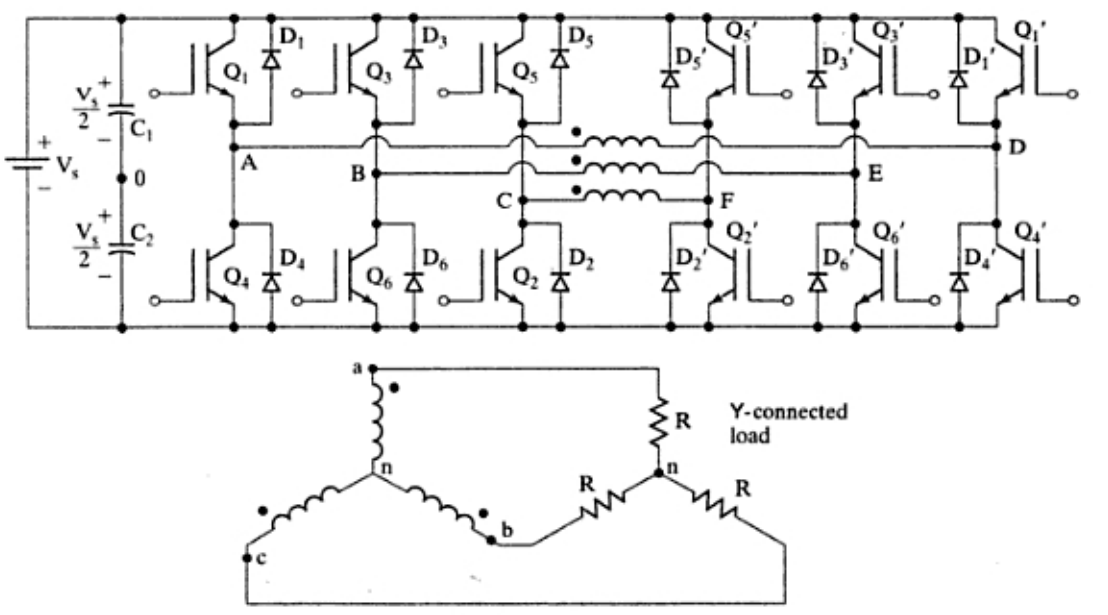
6.5.1 180-Degree Conduction

Each transistor conducts for 180°. Three transistors remain on at any instant of time. When transistor Q_1 is switched on, terminal a is connected to the positive terminal of the dc input voltage. When transistor Q_4 is switched on, terminal a is brought to the negative terminal of the dc source. There are six modes of operation in a cycle and the duration of each mode is 60°. The transistors are numbered in the sequence of gating the transistors (e.g., 123, 234, 345, 456, 561, and 612). The gating signals shown in Figure 6.5b are shifted from each other by 60° to obtain three-phase balanced (fundamental) voltages.

The load may be connected in Y or delta as shown in Figure 6.6. The switches of any leg of the inverter (S_1 and S_4, S_3 and S_6, or S_5 and S_2) cannot be switched on simultaneously; this would result in a short circuit across the dc link voltage supply. Similarly, to avoid undefined states and thus undefined ac output line voltages, the switches of any leg of the inverter cannot be switched off simultaneously; this can result in voltages that depend on the respective line current polarity.



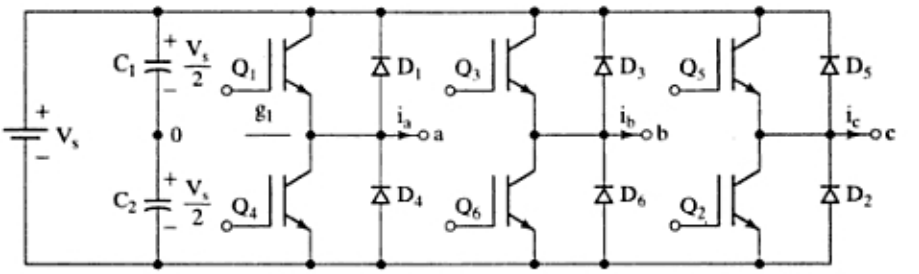
(a) Schematic



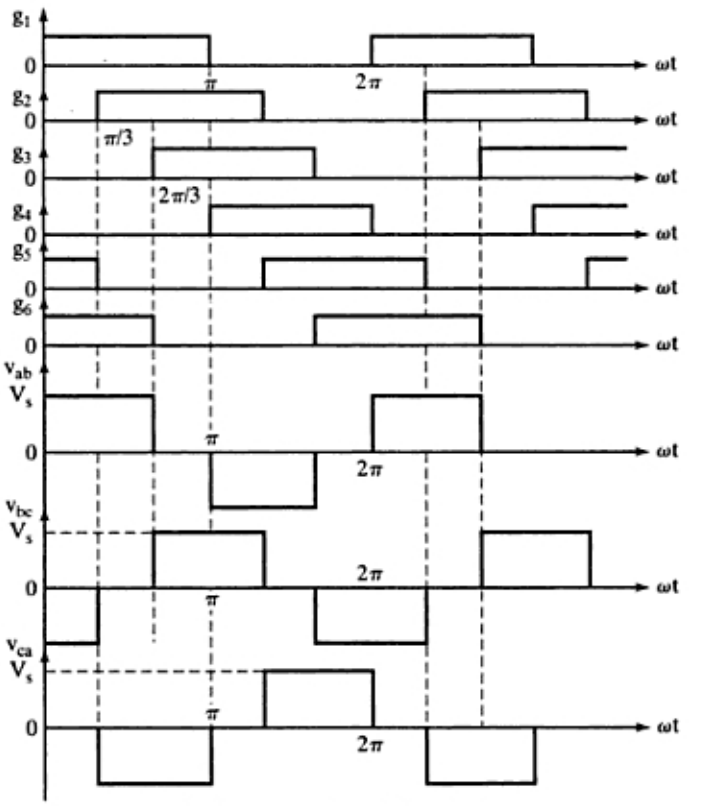
(b) Circuit diagram

FIGURE 6.4

Three-phase inverter formed by three single-phase inverters.



(a) Circuit



(b) Waveforms for 180° conduction

FIGURE 6.5

Three-phase bridge inverter.

Table 6.2 shows eight valid switch states. Transistors $Q1$, $Q6$ in Figure 6.6a act as the switching devices $S1$, $S6$, respectively. If two switches: one upper and one lower conduct at the same time such that the output voltage is $\pm V_s$, the switch state is 1, whereas if these switches are off at the same time, the switch state is 0. States 1 to 6 produce nonzero output voltages. States 7 and 8 produce zero line voltages and the line currents freewheel through either the upper or the lower freewheeling diodes. To

TABLE 6.2 Switch States for Three-Phase Voltage-Source Inverter (VSI)

State	State No.	Switch States	v_{ab}	v_{bc}	v_{ca}	Space Vector
S_1, S_2, and S_6 are on and S_4, S_5, and S_3 are off	1	100	V_S	0	$-V_S$	$\mathbf{V_1} = 1 + j0.577 = 2/\sqrt{3}\ \angle 30°$
S_2, S_3, and S_1 are on and S_5, S_6, and S_4 are off	2	110	0	V_S	$-V_S$	$\mathbf{V_2} = j1.155 = 2/\sqrt{3}\ \angle 90°$
S_3, S_4, and S_2 are on and S_6, S_1, and S_5 are off	3	010	$-V_S$	V_S	0	$\mathbf{V_3} = -1 + j0.577 = 2/\sqrt{3}\ \angle 150°$
S_4, S_5, and S_3 are on and S_1, S_2, and S_6 are off	4	011	$-V_S$	0	V_S	$\mathbf{V_4} = -1 - j0.577 = 2/\sqrt{3}\ \angle 210°$
S_5, S_6, and S_4 are on and S_2, S_3, and S_1 are off	5	001	0	$-V_S$	V_S	$\mathbf{V_5} = -j1.155 = 2/\sqrt{3}\ \angle 270°$
S_6, S_1, and S_5 are on and S_3, S_4, and S_2 are off	6	101	V_S	$-V_S$	0	$\mathbf{V_6} = 1 - j0.577 = 2/\sqrt{3}\ \angle 330°$
S_1, S_3, and S_5 are on and S_4, S_6, and S_2 are off	7	111	0	0	0	$\mathbf{V_7} = 0$
S_4, S_6, and S_2 are on and S_1, S_3, and S_5 are off	8	000	0	0	0	$\mathbf{V_0} = 0$

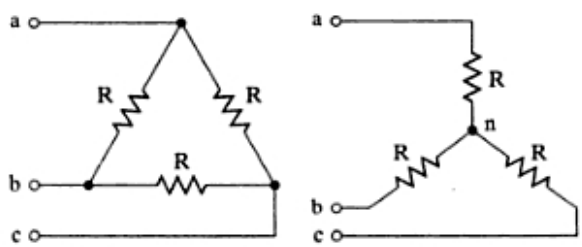
generate a given voltage waveform, the inverter moves from one state to another. Thus, the resulting ac output line voltages are built up of discrete values of voltages of V_s, 0, and $-V_s$. To generate the given waveform, the selection of the states is usually done by a modulating technique that should assure the use of only the valid states.

For a delta-connected load, the phase currents can be obtained directly from the line-to-line voltages. Once the phase currents are known, the line currents can be determined. For a Y-connected load, the line-to-neutral voltages must be determined to find the line (or phase) currents. There are three modes of operation in a half-cycle and the equivalent circuits are shown in Figure 6.7a for a Y-connected load.

During mode 1 for $0 \le \omega t < \pi/3$, transistors Q_1, Q_5, and Q_6 conduct

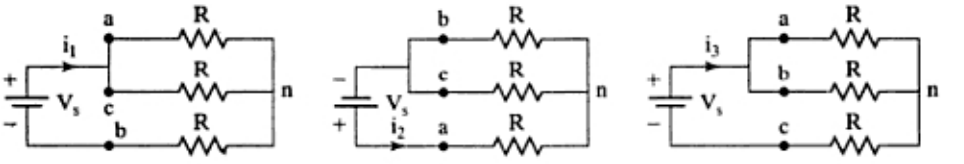
$$R_{eq} = R + \frac{R}{2} = \frac{3R}{2}$$

$$i_1 = \frac{V_s}{R_{eq}} = \frac{2V_s}{3R}$$

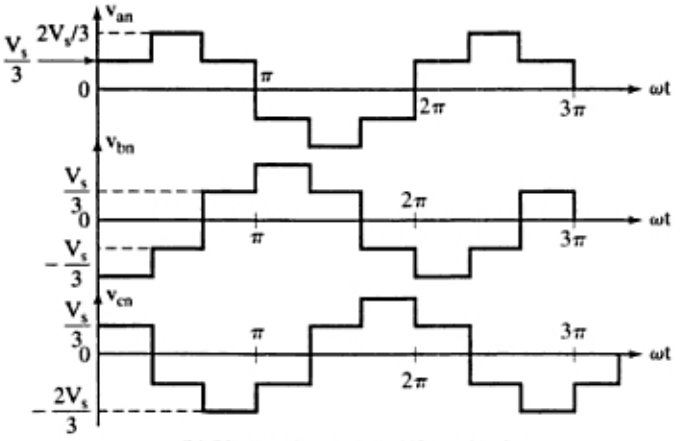


(a) Delta connected (b) Y-connected

FIGURE 6.6
Delta- and Y-connected load.



(a) Equivalent circuits



(b) Phase voltages for 180° conduction

FIGURE 6.7

Equivalent circuits for Y-connected resistive load.

$$v_{an} = v_{cn} = \frac{i_1 R}{2} = \frac{V_s}{3}$$

$$v_{bn} = -i_1 R = \frac{-2V_s}{3}$$

During mode 2 for $\pi/3 \leq \omega t < 2\pi/3$, transistors Q_1, Q_2, and Q_6 conduct

$$R_{eq} = R + \frac{R}{2} = \frac{3R}{2}$$

$$i_2 = \frac{V_s}{R_{eq}} = \frac{2V_s}{3R}$$

$$v_{an} = i_2 R = \frac{2V_s}{3}$$

$$v_{bn} = v_{cn} = \frac{-i_2 R}{2} = \frac{-V_s}{3}$$

During mode 3 for $2\pi/3 \leq \omega t < \pi$, transistors Q_1, Q_2, and Q_3 conduct

$$R_{eq} = R + \frac{R}{2} = \frac{3R}{2}$$

$$i_3 = \frac{V_s}{R_{eq}} = \frac{2V_s}{3R}$$

$$v_{an} = v_{bn} = \frac{i_3 R}{2} = \frac{V_s}{3}$$

$$v_{cn} = i_3 R = \frac{-2V_s}{3}$$

The line-to-neutral voltages are shown in Figure 6.7b. The instantaneous line-to-line voltage v_{ab} in Figure 6.5b can be expressed in a Fourier series,

$$v_{ab} = \frac{a_0}{2} + \sum_{n=1}^{\infty} (a_n \cos(n\omega t) + b_n \sin(n\omega t))$$

Due to the quarter-wave symmetry along the x-axis, both a_0 and a_n are zero. Assuming symmetry along the y-axis at $\omega t = \pi/6$, we can write b_n as

$$b_n = \frac{1}{\pi}\left[\int_{-5\pi/6}^{-\pi/6} -V_s d(\omega t) + \int_{\pi/6}^{5\pi/6} V_s d(\omega t)\right] = \frac{4V_s}{n\pi} \sin\left(\frac{n\pi}{2}\right) \sin\left(\frac{n\pi}{3}\right)$$

which, recognizing that v_{ab} is phase shifted by $\pi/6$ and the even harmonics are zero, gives the instantaneous line-to-line voltage v_{ab} (for a Y-connected load) as

$$v_{ab} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_s}{n\pi} \sin\frac{n\pi}{3} \sin n\left(\omega t + \frac{\pi}{6}\right) \tag{6.16a}$$

Both v_{bc} and v_{ca} can be found from Eq. (6.16a) by phase shifting v_{ab} by 120° and 240°, respectively,

$$v_{bc} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_s}{n\pi} \sin\frac{n\pi}{3} \sin n\left(\omega t - \frac{\pi}{2}\right) \tag{6.16b}$$

$$v_{ca} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_s}{n\pi} \sin\frac{n\pi}{3} \sin n\left(\omega t - \frac{7\pi}{6}\right) \tag{6.16c}$$

We can notice from Eqs. (6.16a) to (6.16c) that the triplen harmonics ($n = 3, 9, 15, \ldots$) would be zero in the line-to-line voltages.

The line-to-line rms voltage can be found from

$$V_L = \left[\frac{2}{2\pi}\int_0^{2\pi/3} V_s^2 \, d(\omega t)\right]^{1/2} = \sqrt{\frac{2}{3}} V_s = 0.8165 V_s \tag{6.17}$$

From Eq. (6.16a), the rms nth component of the line voltage is

$$V_{Ln} = \frac{4V_s}{\sqrt{2}n\pi} \sin\frac{n\pi}{3} \tag{6.18}$$

which, for $n = 1$, gives the rms fundamental line voltage.

$$V_{L1} = \frac{4V_s \sin 60°}{\sqrt{2}\pi} = 0.7797V_s \tag{6.19}$$

The rms value of line-to-neutral voltages can be found from the line voltage,

$$V_p = \frac{V_L}{\sqrt{3}} = \frac{\sqrt{2}\,V_s}{3} = 0.4714V_s \tag{6.20}$$

With resistive loads, the diodes across the transistors have no functions. If the load is inductive, the current in each arm of the inverter would be delayed to its voltage as shown in Figure 6.8. When transistor Q_4 in Figure 6.5a is off, the only path for the negative line current i_a is through D_1. Hence, the load terminal a is connected to the dc source through D_1 until the load current reverses its polarity at $t = t_1$. During the period for $0 \le t \le t_1$, transistor Q_1 cannot conduct. Similarly, transistor Q_4 only starts to conduct at $t = t_2$. The transistors must be continuously gated, because the conduction time of transistors and diodes depends on the load power factor.

For a Y-connected load, the phase voltage is $v_{an} = v_{ab}/\sqrt{3}$ with a delay of 30° with respect to v_{ab}. Therefore, the instantaneous phase voltages (for a Y-connected load) are

$$v_{aN} = \sum_{n=1}^{\infty} \frac{4V_s}{\sqrt{3}n\pi} \sin\left(\frac{n\pi}{3}\right) \sin(n\omega t) \qquad \text{for } n = 1, 3, 5, \ldots \tag{6.21a}$$

$$v_{bN} = \sum_{n=1}^{\infty} \frac{4V_s}{\sqrt{3}n\pi} \sin\left(\frac{n\pi}{3}\right) \sin n\left(\omega t - \frac{2\pi}{3}\right) \qquad \text{for } n = 1, 3, 5, \ldots \tag{6.21b}$$

$$v_{bN} = \sum_{n=1}^{\infty} \frac{4V_s}{\sqrt{3}n\pi} \sin\left(\frac{n\pi}{3}\right) \sin n\left(\omega t - \frac{4\pi}{3}\right) \qquad \text{for } n = 1, 3, 5, \ldots \tag{6.21c}$$

Dividing the instantaneous phase voltage v_{aN} by the load impedance,

$$Z = R + jn\omega L$$

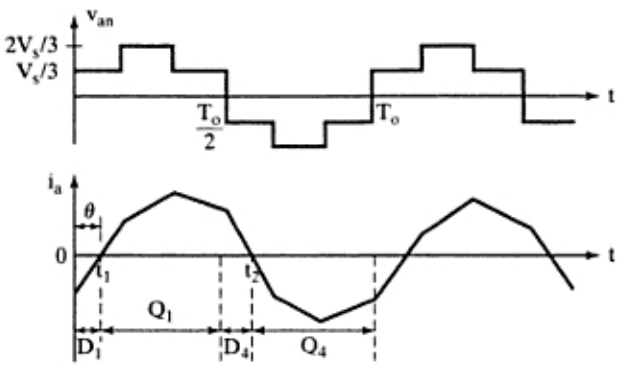


FIGURE 6.8

Three-phase inverter with *RL* load.

Using Eq. (6.21a), the line current i_a for an RL load is given by

$$i_a = \sum_{n=1,3,5,\ldots}^{\infty} \left[\frac{4V_s}{\sqrt{3}[n\pi\sqrt{R^2 + (n\omega L)^2}]} \sin\frac{n\pi}{3} \right] \sin(n\omega t - \theta_n) \qquad (6.22)$$

where $\theta_n = \tan^{-1}(n\omega L/R)$.

Note: For a delta-connected load, the phase voltages (v_{aN}, v_{bN}, and v_{cN}) are the same as the line-to-line voltages (v_{ab}, v_{bc}, and v_{ca}) as shown in Figure 6.6b and as described by Eq. (6.16).

Dc supply current. Neglecting losses, the instantaneous power balance gives

$$v_s(t)i_s(t) = v_{ab}(t)i_a(t) + v_{bc}(t)i_b(t) + v_{ca}(t)i_c(t)$$

where $i_a(t)$, $i_b(t)$, and $i_c(t)$ are the phase currents in a delta-connected load. Assuming that the ac output voltages are sinusoidal and the dc supply voltage is constant $v_s(t) = V_s$, we get the dc supply current

$$i_s(t) = \frac{1}{V_s}\left\{ \begin{array}{l} \sqrt{2}V_{o1}\sin(\omega t) \times \sqrt{2}I_o\sin(\omega t - \theta_1) \\ \quad + \sqrt{2}V_{o1}\sin(\omega t - 120^\circ) \times \sqrt{2}I_o\sin(\omega t - 120^\circ - \theta_1) \\ \quad + \sqrt{2}V_{o1}\sin(\omega t - 240^\circ) \times \sqrt{2}I_o\sin(\omega t - 240^\circ - \theta_1) \end{array} \right\}$$

The dc supply current can be simplified to

$$I_s = 3\frac{V_{o1}}{V_s} I_o \cos(\theta_1) = \sqrt{3}\frac{V_{o1}}{V_s} I_L \cos(\theta_1) \qquad (6.23)$$

where $I_L = \sqrt{3}\, I_o$ is the rms load line current;
V_{o1} is the fundamental rms output line voltage;
I_o is the rms load phase current;
θ_1 is the load impedance angle at the fundamental frequency.

Thus, if the load voltages are harmonic free, the dc supply current becomes harmonic free. However, because the load line voltages contain harmonics, the dc supply current also contains harmonics.

Gating sequence. The gating sequence for switching devices is as follows

1. Generate three square-wave gating-signals v_{g1}, v_{g3}, and v_{g5} at an output frequency f_0 and a 50% duty cycle. Signals v_{g4}, v_{g6}, and v_{g2} should be logic invert signals of v_{g1}, v_{g3}, and v_{g5}, respectively. Each signal is shifted from the other by 60°.
2. Signals v_{g1}, v_{g3}, and v_{g5} drive Q_1, Q_3, and Q_5, respectively, through gate-isolating circuits. Signals v_{g2}, v_{g4}, and v_{g6} can drive Q_2, Q_4, and Q_6, respectively, without any isolating circuits.

Example 6.4 Finding the Output Voltage and Current of a Three-Phase Full-Bridge Inverter with an *RL* load

The three-phase inverter in Figure 6.5a has a Y-connected load of $R = 5\ \Omega$ and $L = 23$ mH. The inverter frequency is $f_0 = 60$ Hz and the dc input voltage is $V_s = 220$ V. (a) Express the instantaneous line-to-line voltage $v_{ab}(t)$ and line current $i_a(t)$ in a Fourier series. Determine (b) the rms line voltage V_L; (c) the rms phase voltage V_p; (d) the rms line voltage V_{L1} at the fundamental

frequency; (e) the rms phase voltage at the fundamental frequency V_{p1}; (f) the THD; (g) the DF; (h) the HF and DF of the LOH; (i) the load power P_o; (j) the average transistor current $I_{Q(av)}$; and (k) the rms transistor current $I_{Q(\text{rms})}$.

Solution

$V_s = 220$ V, $R = 5\ \Omega$, $L = 23$ mH, $f_0 = 60$ Hz, and $\omega = 2\pi \times 60 = 377$ rad/s.

a. Using Eq. (6.16a), the instantaneous line-to-line voltage $v_{ab}(t)$ can be written as

$$\begin{aligned} v_{ab}(t) &= 242.58 \sin(377t + 30°) - 48.52 \sin 5(377t + 30°) \\ &\quad - 34.66 \sin 7(377t + 30°) + 22.05 \sin 11(377t + 30°) \\ &\quad + 18.66 \sin 13(377t + 30°) - 14.27 \sin 17(377t + 30°) + \cdots \end{aligned}$$

$$Z_L = \sqrt{R^2 + (n\omega L)^2}\underline{/\tan^{-1}(n\omega L/R)} = \sqrt{5^2 + (8.67n)^2}\underline{/\tan^{-1}(8.67n/5)}$$

Using Eq. (6.22), the instantaneous line (or phase) current is given by

$$\begin{aligned} i_{a(t)} &= 14 \sin(377t - 60°) - 0.64 \sin(5 \times 377t - 83.4°) \\ &\quad - 0.33 \sin(7 \times 377t - 85.3°) + 0.13 \sin(11 \times 377t - 87°) \\ &\quad + 0.10 \sin(13 \times 377t - 87.5°) - 0.06 \sin(17 \times 377t - 88°) - \cdots \end{aligned}$$

b. From Eq. (6.17), $V_L = 0.8165 \times 220 = 179.63$ V.

c. From Eq. (6.20), $V_p = 0.4714 \times 220 = 103.7$ V.

d. From Eq. (6.19), $V_{L1} = 0.7797 \times 220 = 171.53$ V.

e. $V_{p1} = V_{L1}/\sqrt{3} = 99.03$ V.

f. From Eq. (6.19), $V_{L1} = 0.7797V_S$

$$\left(\sum_{n=5,7,11,\ldots}^{\infty} V_{Ln}^2\right)^{1/2} = (V_L^2 - V_{L1}^2)^{1/2} = 0.24236V_s$$

From Eq. (6.8), THD $= 0.24236V_s/(0.7797V_s) = 31.08\%$. The rms harmonic line voltage is

g. $$V_{Lh} = \left[\sum_{n=5,7,11,\ldots}^{\infty} \left(\frac{V_{Ln}}{n^2}\right)^2\right]^{1/2} = 0.00941V_s$$

From Eq. (6.9), DF $= 0.00941V_s/(0.7797V_s) = 1.211\%$.

h. The LOH is the fifth, $V_{L5} = V_{L1}/5$. From Eq. (6.7), $\text{HF}_5 = V_{L5}/V_{L1} = 1/5 = 20\%$, and from Eq. (6.10), $\text{DF}_5 = (V_{L5}/5^2)/V_{L1} = 1/125 = 0.8\%$.

i. For Y-connected loads, the line current is the same as the phase current and the rms line current,

$$I_L = \frac{(14^2 + 0.64^2 + 0.33^2 + 0.13^2 + 0.10^2 + 0.06^2)^{1/2}}{\sqrt{2}} = 9.91 \text{ A}$$

The load power $P_0 = 3I_L^2R = 3 \times 9.91^2 \times 5 = 1473$ W.

j. The average supply current $I_s = P_o/220 = 1473/220 = 6.7$ A and the average transistor current $I_{Q(av)} = 6.7/3 = 2.23$ A.

k. Because the line current is shared by three transistors, the rms value of a transistor current is $I_{Q(\text{rms})} = I_L/\sqrt{3} = 9.91/\sqrt{3} = 5.72$ A.

6.5.2 120-Degree Conduction

In this type of control, each transistor conducts for 120°. Only two transistors remain on at any instant of time. The gating signals are shown in Figure 6.9. The conduction sequence of transistors is 61, 12, 23, 34, 45, 56, 61. There are three modes of operation in one half-cycle and the equivalent circuits for a Y-connected load are shown in Figure 6.10. During mode 1 for $\leq \omega t \leq \pi/3$, transistors 1 and 6 conduct.

$$v_{an} = \frac{V_s}{2} \qquad v_{bn} = -\frac{V_s}{2} \qquad v_{cn} = 0$$

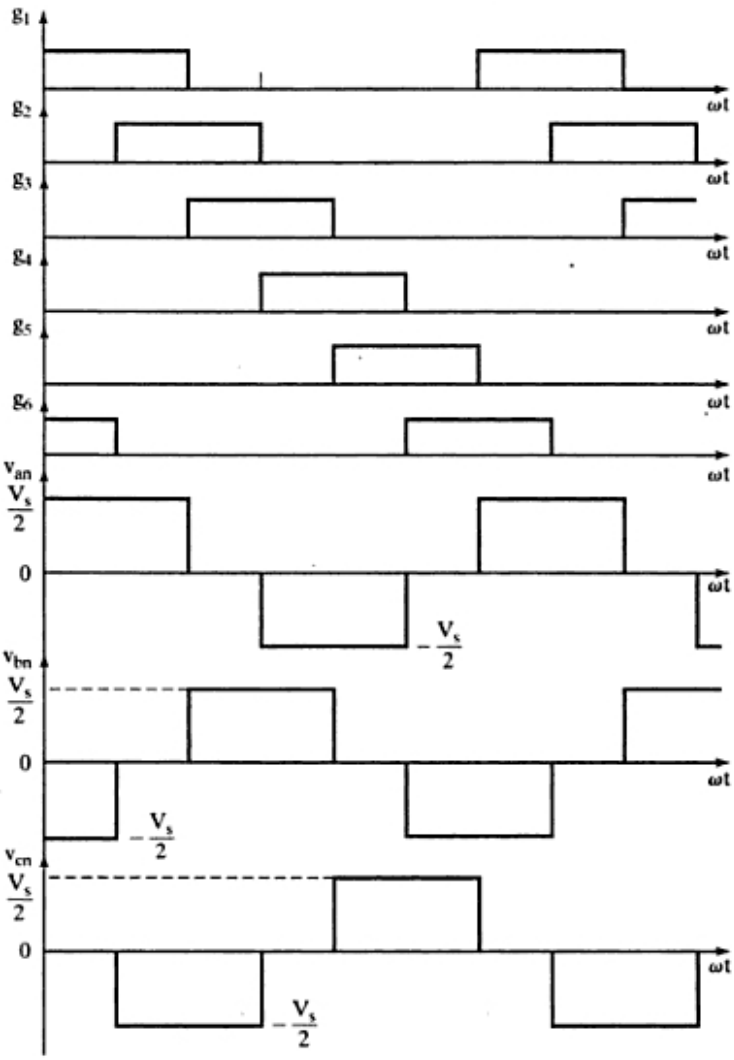


FIGURE 6.9

Gating signals for 120° conduction.

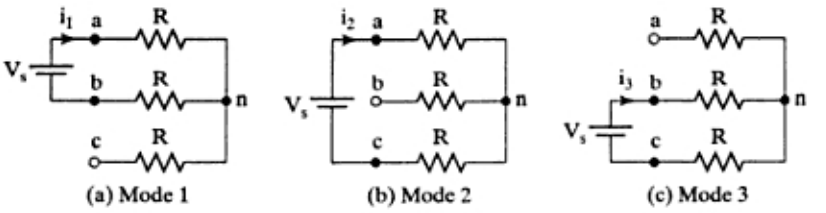


FIGURE 6.10

Equivalent circuits for Y-connected resistive load.

During mode 2 for $\pi/3 \leq \omega t \leq 2\pi/3$, transistors 1 and 2 conduct.

$$v_{an} = \frac{V_s}{2} \qquad v_{bn} = 0 \qquad v_{cn} = -\frac{V_s}{2}$$

During mode 3 for $2\pi/3 \leq \omega t \leq 3\pi/3$, transistors 2 and 3 conduct.

$$v_{an} = 0 \qquad v_{bn} = \frac{V_s}{2} \qquad v_{cn} = -\frac{V_s}{2}$$

The line-to-neutral voltages that are shown in Figure 6.9 can be expressed in Fourier series as

$$v_{an} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2V_s}{n\pi} \sin\frac{n\pi}{3} \sin n\left(\omega t + \frac{\pi}{6}\right) \tag{6.24a}$$

$$v_{bn} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2V_s}{n\pi} \sin\frac{n\pi}{3} \sin n\left(\omega t - \frac{\pi}{2}\right) \tag{6.24b}$$

$$v_{cn} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2V_s}{n\pi} \sin\frac{n\pi}{3} \sin n\left(\omega t - \frac{7\pi}{6}\right) \tag{6.24c}$$

The line a-to-b voltage is $v_{ab} = \sqrt{3}\, v_{an}$ with a phase advance of 30°. Therefore, the instantaneous line-to-line voltages (for a Y-connected load) are

$$v_{ab} = \sum_{n=1}^{\infty} \frac{2\sqrt{3}V_S}{n\pi} \sin\left(\frac{n\pi}{3}\right) \sin n\left(\omega t + \frac{\pi}{3}\right) \quad \text{for } n = 1, 3, 5, \ldots \tag{6.25a}$$

$$v_{bc} = \sum_{n=1}^{\infty} \frac{2\sqrt{3}V_S}{n\pi} \sin\left(\frac{n\pi}{3}\right) \sin n\left(\omega t - \frac{\pi}{3}\right) \quad \text{for } n = 1, 3, 5, \ldots \tag{6.25b}$$

$$v_{ca} = \sum_{n=1}^{\infty} \frac{2\sqrt{3}V_S}{n\pi} \sin\left(\frac{n\pi}{3}\right) \sin n\,(\omega t - \pi) \quad \text{for } n = 1, 3, 5, \ldots \tag{6.25c}$$

There is a delay of $\pi/6$ between the turning off Q_1 and turning on Q_4. Thus, there should be no short circuit of the dc supply through one upper and one lower transistors. At any time, two load terminals are connected to the dc supply and the third one remains open. The potential of this open terminal depends on the load characteristics and would be unpredictable. Because one transistor conducts for 120°, the transistors

are less utilized as compared with those of 180° conduction for the same load condition. Thus, the 180° conduction is preferred and it is generally used in three-phase inverters.

Key Points of Section 6.5

- The three-phase bridge inverter requires six switching devices and six diodes. The rms fundamental component V_{L1} of the output line voltage is $0.7798V_s$ and that for phase voltage is $V_{p1} = V_{L1}/\sqrt{3} = 0.45V_s$ for 180° conduction. For 120° conduction, $V_{P1} = 0.3898V_s$ and $V_{L1} = \sqrt{3}\,V_{P1} = 0.6753V_s$. The 180° conduction is the preferred control method.
- The design of an inverter requires the determination of the average, rms, and peak currents of the switching devices and diodes.

6.6 VOLTAGE CONTROL OF SINGLE-PHASE INVERTERS

In many industrial applications, to control of the output voltage of inverters is often necessary (1) to cope with the variations of dc input voltage, (2) to regulate voltage of inverters, and (3) to satisfy the constant volts and frequency control requirement. There are various techniques to vary the inverter gain. The most efficient method of controlling the gain (and output voltage) is to incorporate PWM control within the inverters. The commonly used techniques are:

1. Single-pulse-width modulation.
2. Multiple-pulse-width modulation.
3. Sinusoidal pulse-width modulation.
4. Modified sinusoidal pulse-width modulation.
5. Phase-displacement control.

6.6.1 Single-Pulse-Width Modulation

In single-pulse-width modulation control, there is only one pulse per half-cycle and the width of the pulse is varied to control the inverter output voltage. Figure 6.11 shows the generation of gating signals and output voltage of single-phase full-bridge inverters. The gating signals are generated by comparing a rectangular reference signal of amplitude A_r with a triangular carrier wave of amplitude A_c. The frequency of the reference signal determines the fundamental frequency of output voltage. The instantaneous output voltage is $v_o = V_s(g_1 - g_4)$. The ratio of A_r to A_c is the control variable and defined as the amplitude *modulation index*. The amplitude modulation index, or simply modulation index

$$M = \frac{A_r}{A_c} \tag{6.26}$$

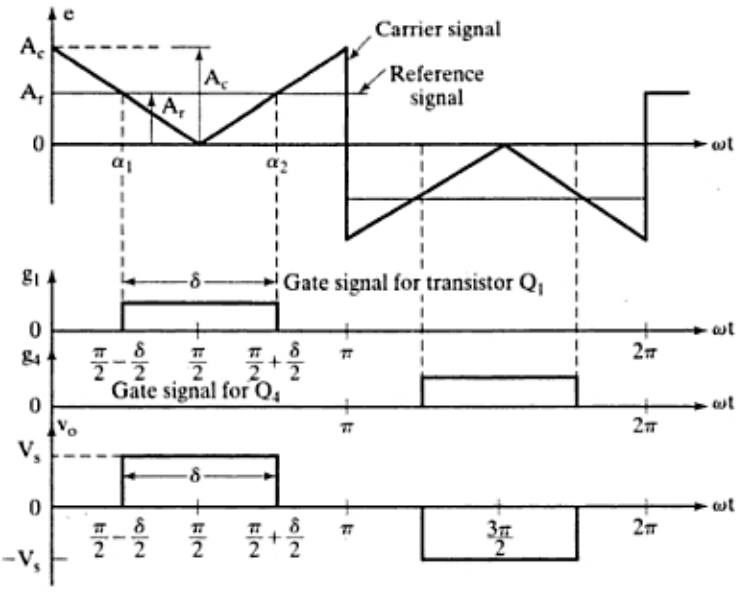


FIGURE 6.11

Single pulse-width modulation.

The rms output voltage can be found from

$$V_o = \left[\frac{2}{2\pi}\int_{(\pi-\delta)/2}^{(\pi+\delta)/2} V_s^2\, d(\omega t)\right]^{1/2} = V_s\sqrt{\frac{\delta}{\pi}} \tag{6.27}$$

By varying A_r from 0 to A_c, the pulse width δ can be modified from 0° to 180° and the rms output voltage V_o, from 0 to V_s.

The Fourier series of output voltage yields

$$v_o(t) = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_s}{n\pi}\sin\frac{n\delta}{2}\sin n\omega t \tag{6.28}$$

Due to the symmetry of the output voltage along the x-axis, the even harmonics (for $n = 2, 4, 6, \ldots$) are absent. A computer program is developed to evaluate the performance of single-pulse modulation for single-phase full-bridge inverters. Figure 6.12 shows the harmonic profile with the variation of modulation index M. The dominant harmonic is the third, and the DF increases significantly at a low output voltage.

The time and angles of intersections can be found from

$$t_1 = \frac{\alpha_1}{\omega} = (1 - M)\frac{T_S}{2} \tag{6.29a}$$

$$t_2 = \frac{\alpha_2}{\omega} = (1 + M)\frac{T_S}{2} \tag{6.29b}$$

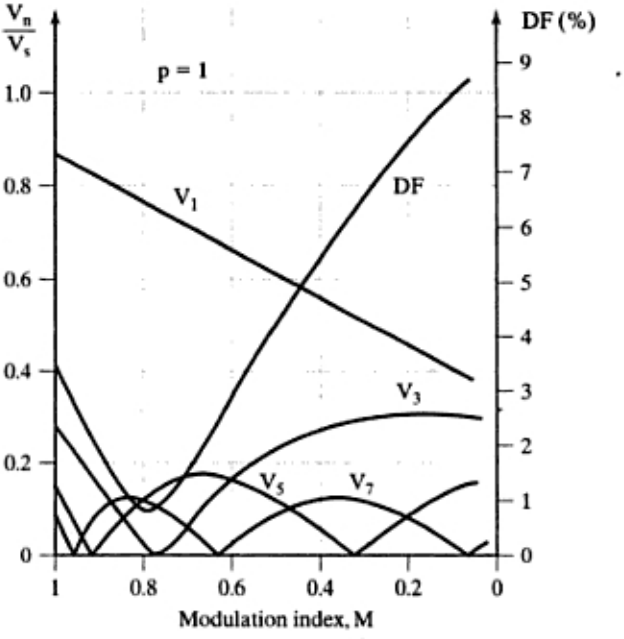


FIGURE 6.12

Harmonic profile of single-pulse-width modulation.

which gives the pulse width d (or pulse angle δ) as

$$d = \frac{\delta}{\omega} = t_2 - t_1 = MT_s \tag{6.29c}$$

where $T_s = T/2$.

Gating sequence. The algorithm for generating the gating signals are as follows:

1. Generate a triangular carrier signal v_{cr} of switching period $T_s = T/2$. Compare v_{cr} with a dc reference signal v_r to produce the difference $v_e = v_{cr} - v_r$, which must pass through a gain limiter to produce a square wave of width d at a switching period T_s.
2. To produce the gating signal g_1, multiply the resultant square wave by a unity signal v_z, which must be a unity pulse of 50% duty cycle at a period of T.
3. To produce the gating signal g_2, multiply the square wave by a logic-invert signal of v_z.

6.6.2 Multiple-Pulse-Width Modulation

The harmonic content can be reduced by using several pulses in each half-cycle of output voltage. The generation of gating signals (in Figure 6.13b) for turning on and off of transistors is shown in Figure 6.13a by comparing a reference signal with a triangular carrier wave. The gate signals are shown in Figure 6.13b. The frequency of reference

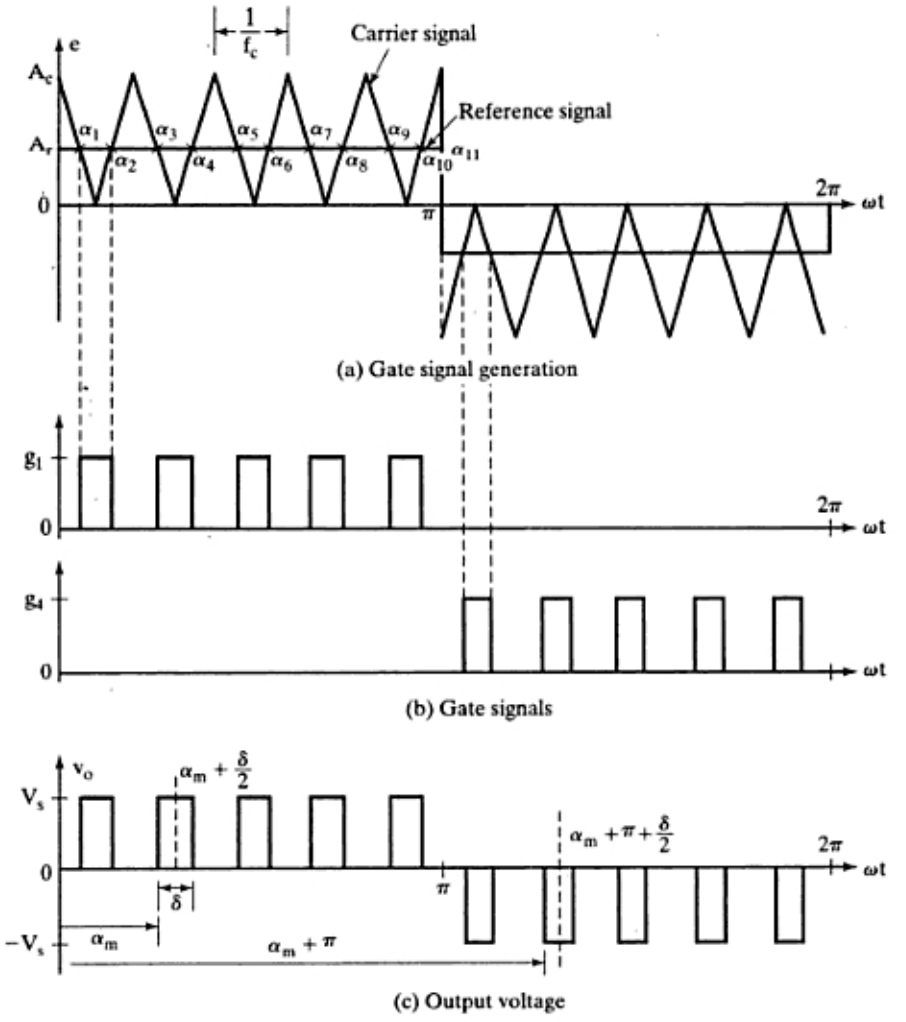


FIGURE 6.13
Multiple-pulse-width modulation.

signal sets the output frequency f_o, and the carrier frequency f_c determines the number of pulses per half-cycle p. The modulation index controls the output voltage. This type of modulation is also known as *uniform pulse-width modulation* (UPWM). The number of pulses per half-cycle is found from

$$p = \frac{f_c}{2f_o} = \frac{m_f}{2} \tag{6.30}$$

where $m_f = f_c/f_o$ is defined as the *frequency modulation ratio.*

The instantaneous output voltage is $v_o = V_s(g_1 - g_4)$. The output voltage for single-phase bridge inverters is shown in Figure 6.13c for UPWM.

If δ is the width of each pulse, the rms output voltage can be found from

$$V_o = \left[\frac{2p}{2\pi}\int_{(\pi/p-\delta)/2}^{(\pi/p+\delta)/2} V_s^2\, d(\omega t)\right]^{1/2} = V_s\sqrt{\frac{p\delta}{\pi}} \tag{6.31}$$

The variation of the modulation index M from 0 to 1 varies the pulse width d from 0 to $T/2p$ (0 to π/p) and the rms output voltage V_o from 0 to V_s. The general form of a Fourier series for the instantaneous output voltage is

$$v_o(t) = \sum_{n=1,3,5,\ldots}^{\infty} B_n \sin n\omega t \tag{6.32}$$

The coefficient B_n in Eq. (6.32) can be determined by considering a pair of pulses such that the positive pulse of duration δ starts at $\omega t = \alpha$ and the negative one of the same width starts at $\omega t = \pi + \alpha$. This is shown in Figure 6.13c. The effects of all pulses can be combined together to obtain the effective output voltage.

If the positive pulse of mth pair starts at $\omega t = \alpha_m$, and ends at $\omega t = \alpha_m + \delta$, the Fourier coefficient for a pair of pulses is

$$\begin{aligned} b_n &= \frac{2}{\pi}\left[\int_{\alpha_m+\delta/2}^{\alpha_m+\delta} \sin n\omega t\, d(\omega t) - \int_{\pi+\alpha_m}^{\pi+\alpha_m+\delta/2} \sin n\omega t\, d(\omega t)\right] \\ &= \frac{4V_s}{n\pi}\sin\frac{n\delta}{4}\left[\sin n\left(\alpha_m + \frac{3\delta}{4}\right) - \sin n\left(\pi + \alpha_m + \frac{\delta}{4}\right)\right] \end{aligned} \tag{6.33}$$

The coefficient B_n of Eq. (6.32) can be found by adding the effects of all pulses,

$$B_n = \sum_{m=1}^{2p} \frac{4V_s}{n\pi}\sin\frac{n\delta}{4}\left[\sin n\left(\alpha_m + \frac{3\delta}{4}\right) - \sin n\left(\pi + \alpha_m + \frac{\delta}{4}\right)\right] \tag{6.34}$$

A computer program is used to evaluate the performance of multiple pulse modulation. Figure 6.14 shows the harmonic profile against the variation of modulation index for five pulses per half-cycle. The order of harmonics is the same as that of single-pulse modulation. The distortion factor is reduced significantly compared with that of single-pulse modulation. However, due to larger number of switching on and off processes of power transistors, the switching losses would increase. With larger values of p, the amplitudes of LOH would be lower, but the amplitudes of some higher order harmonics would increase. However, such higher order harmonics produce negligible ripple or can easily be filtered out.

Due to the symmetry of the output voltage along the x-axis, $A_n = 0$ and the even harmonics (for $n = 2, 4, 6, \ldots$) are absent.

The mth time t_m and angle α_m of intersection can be determined from

$$t_m = \frac{\alpha_m}{\omega} = (m - M)\frac{T_s}{2} \qquad \text{for} \qquad m = 1, 3, \ldots, 2p \tag{6.35a}$$

$$t_m = \frac{\alpha_m}{\omega} = (m - 1 + M)\frac{T_s}{2} \qquad \text{for} \qquad m = 2, 4, \ldots, 2p \tag{6.35b}$$

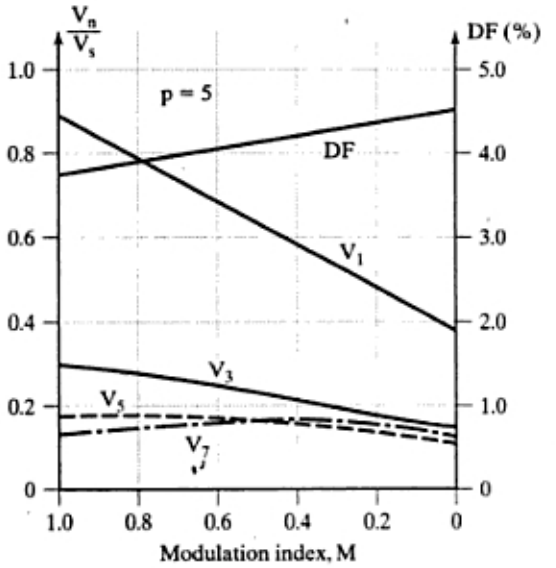


FIGURE 6.14
Harmonic profile of multiple-pulse-width modulation.

Because all widths are the same, we get the pulse width d (or pulse angle δ) as

$$d = \frac{\delta}{\omega} = t_{m+1} - t_m = MT_s \tag{6.35c}$$

where $T_s = T/2p$.

The algorithm for generating the gating signals is the same as that for single-pulse modulation, except the switching period T_s of the triangular carrier signal v_{cr} is $T/2p$ instead of $T/2$.

6.6.3 Sinusoidal Pulse-Width Modulation

Instead of maintaining the width of all pulses the same as in the case of multiple-pulse modulation, the width of each pulse is varied in proportion to the amplitude of a sine wave evaluated at the center of the same pulse [2]. The DF and LOH are reduced significantly. The gating signals as shown in Figure 6.15a are generated by comparing a sinusoidal reference signal with a triangular carrier wave of frequency f_c. This sinusoidal pulse-width modulation (SPWM) is commonly used in industrial applications. The frequency of reference signal f_r determines the inverter output frequency f_o; and its peak amplitude A_r controls the modulation index M, and then in turn the rms output voltage V_o. Comparing the bidirectional carrier signal v_{cr} with two sinusoidal reference signals v_r and $-v_r$ shown in Figure 6.15a produces gating signals g_1 and g_4, respectively, as shown in Figure 6.15b. The output voltage is $v_o = V_s(g_1 - g_4)$. However, g_1 and g_4 cannot be released at the same time. The number of pulses per half-cycle depends on the carrier frequency. Within the constraint that two transistors of the same arm (Q_1 and

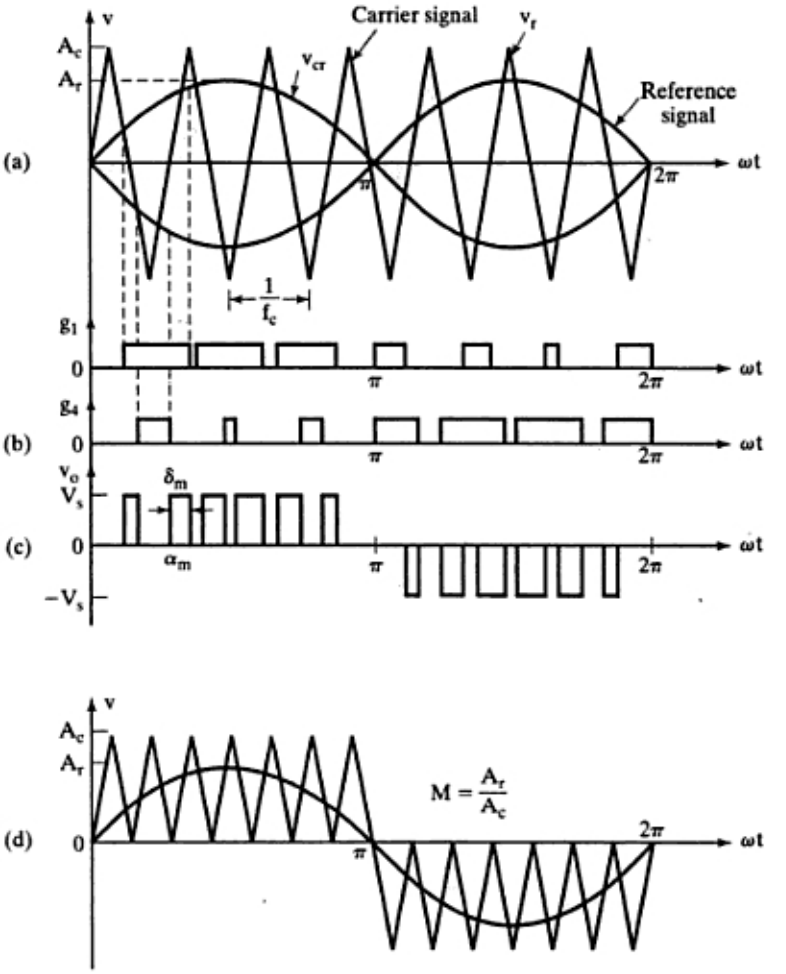


FIGURE 6.15

Sinusoidal pulse-width modulation.

Q_4) cannot conduct at the same time, the instantaneous output voltage is shown in Figure 6.15c. The same gating signals can be generated by using unidirectional triangular carrier wave as shown in Figure 6.15d. It is easier to implement this method and is preferable. The algorithm for generating the gating signals is similar to that for the uniform PWM in Section 6.6.2, except the reference signal is a sine wave $v_r = V_r \sin \omega t$, instead of a dc signal. The output voltage is $v_o = V_s(g_1 - g_4)$.

The rms output voltage can be varied by varying the modulation index M. It can be observed that the area of each pulse corresponds approximately to the area under the sine wave between the adjacent midpoints of off periods on the gating signals. If δ_m is the width of mth pulse, Eq. (6.31) can be extended to find the rms output voltage

$$V_o = V_s \left(\sum_{m=1}^{2p} \frac{\delta_m}{\pi} \right)^{1/2} \tag{6.36}$$

Equation (6.34) can also be applied to determine the Fourier coefficient of output voltage as

$$B_n = \sum_{m=1}^{2p} \frac{4V_s}{n\pi} \sin\frac{n\delta_m}{4}\left[\sin n\left(\alpha_m + \frac{3\delta_m}{4}\right) - \sin n\left(\pi + \alpha_m + \frac{\delta_m}{4}\right)\right] \quad \text{for } n = 1, 3, 5, \ldots \tag{6.37}$$

A computer program is developed to determine the width of pulses and to evaluate the harmonic profile of sinusoidal modulation. The harmonic profile is shown in Figure 6.16 for five pulses per half-cycle. The DF is significantly reduced compared with that of multiple-pulse modulation. This type of modulation eliminates all harmonics less than or equal to $2p - 1$. For $p = 5$, the LOH is ninth.

The mth time t_m and angle α_m of intersection can be determined from

$$t_m = \frac{\alpha_m}{\omega} = t_x + m\frac{T_s}{2} \tag{6.38a}$$

where t_x can be solved from

$$1 - \frac{2t}{T_s} = M \sin\left[\omega\left(t_x + \frac{mT_s}{2}\right)\right] \quad \text{for} \quad m = 1, 3, \ldots, 2p \tag{6.38b}$$

$$\frac{2t}{T_s} = M \sin\left[\omega\left(t_x + \frac{mT_s}{2}\right)\right] \quad \text{for} \quad m = 2, 4, \ldots, 2p \tag{6.38c}$$

where $T_s = T/2(p + 1)$. The width of the mth pulse d_m (or pulse angle δ_m) can be found from

$$d_m = \frac{\delta_m}{\omega} = t_{m+1} - t_m \tag{6.38d}$$

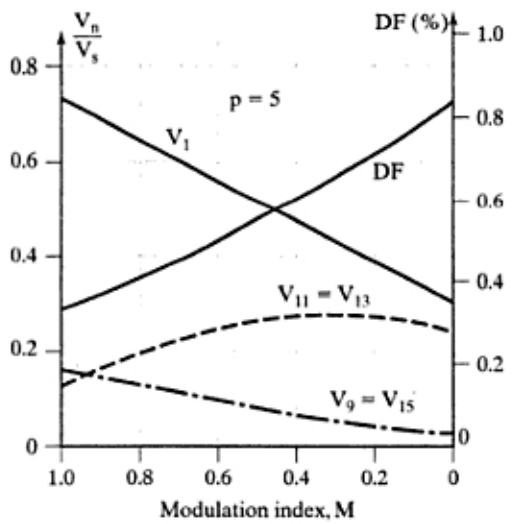


FIGURE 6.16
Harmonic profile of sinusoidal pulse-width modulation.

The output voltage of an inverter contains harmonics. The PWM pushes the harmonics into a high-frequency range around the switching frequency f_c and its multiples, that is, around harmonics m_f, $2m_f$, $3m_f$, and so on. The frequencies at which the voltage harmonics occur can be related by

$$f_n = (jm_f \pm k)f_c \tag{6.39}$$

where the nth harmonic equals the kth sideband of jth times the frequency to modulation ratio m_f.

$$\begin{aligned} n &= jm_f \pm k \\ &= 2jp \pm k \qquad \text{for } j = 1, 2, 3, \ldots \text{ and } k = 1, 3, 5, \ldots \end{aligned} \tag{6.40}$$

The peak fundamental output voltage for PWM and SPWM control can be found approximately from

$$V_{m1} = dV_s \qquad \text{for } 0 \le d \le 1.0 \tag{6.41}$$

For $d = 1$, Eq. (6.41) gives the maximum peak amplitude of the fundamental output voltage as $V_{m1(\max)} = V_s$. According to Eq. (6.12), $V_{m1(\max)}$ could be as high as $4V_s/\pi = 1.273V_s$ for a square-wave output. To increase the fundamental output voltage, d must be increased beyond 1.0. The operation beyond $d = 1.0$ is called *overmodulation*. The value of d at which $V_{m1(\max)}$ equals $1.273V_s$ is dependent on the number of pulses per half-cycle p and is approximately 3 for $p = 7$, as shown in Figure 6.17. Overmodulation basically leads to a square-wave operation and adds more harmonics as compared with operation in the linear range (with $d \le 1.0$). Overmodulation is normally avoided in applications requiring low distortion (e.g., uninterruptible power supplies [UPSs]).

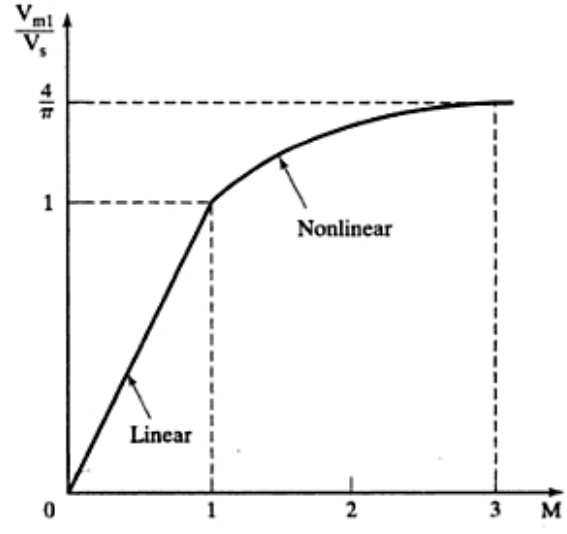


FIGURE 6.17

Peak fundamental output voltage versus modulation index M.

6.6.4 Modified Sinusoidal Pulse-Width Modulation

Figure 6.15c indicates that the widths of pulses nearer the peak of the sine wave do not change significantly with the variation of modulation index. This is due to the characteristics of a sine wave, and the SPWM technique can be modified so that the carrier wave is applied during the first and last 60° intervals per half-cycle (e.g., 0° to 60° and 120° to 180°). This modified sinusoidal pulse-width modulation (MSPWM) is shown in Figure 6.18. The fundamental component is increased and its harmonic characteristics are improved. It reduces the number of switching of power devices and also reduces switching losses.

The mth time t_m and angle α_m of intersection can be determined from

$$t_m = \frac{\alpha_m}{\omega} = t_x + m\frac{T_s}{2} \qquad \text{for } m = 1, 2, 3, \ldots, p \tag{6.42a}$$

where t_x can be solved from

$$1 - \frac{2t}{T_s} = M \sin\left[\omega\left(t_x + \frac{mT_s}{2}\right)\right] \qquad \text{for } m = 1, 3, \ldots, p \tag{6.42b}$$

$$\frac{2t}{T_s} = M \sin\left[\omega\left(t_x + \frac{mT_s}{2}\right)\right] \qquad \text{for } m = 2, 4, \ldots, p \tag{6.42c}$$

The time intersections during the last 60° intervals can be found from

$$t_{m+1} = \frac{\alpha_{m+1}}{\omega} = \frac{T}{2} - t_{2p-m} \qquad \text{for } m = p, p+1 \ldots, 2p-1 \tag{6.42d}$$

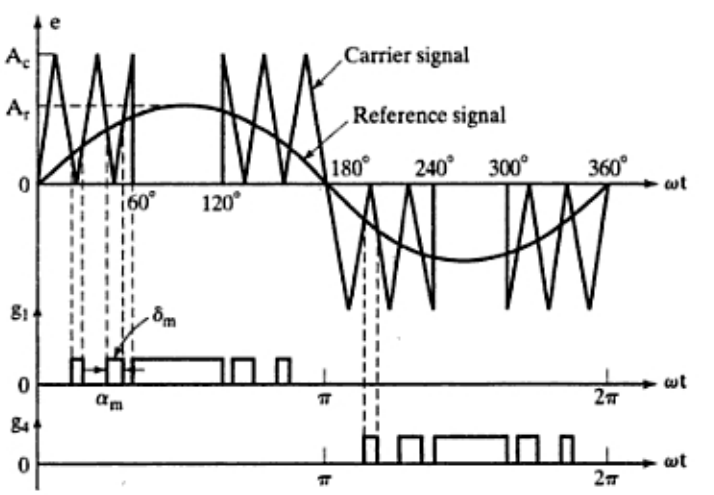


FIGURE 6.18
Modified sinusoidal pulse-width modulation.

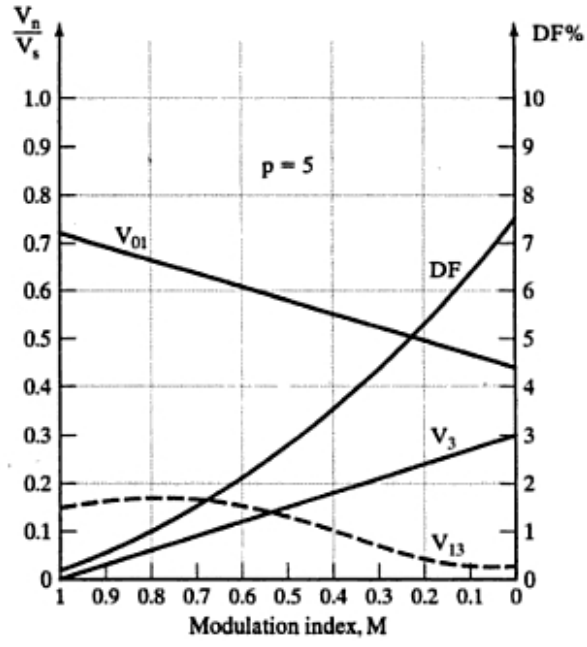


FIGURE 6.19

Harmonic profile of modified sinusoidal pulse-width modulation.

where $T_s = T/6(p + 1)$. The width of the mth pulse d_m (or pulse angle δ_m) can be found from

$$d_m = \frac{\delta_m}{\omega} = t_{m+1} - t_m \tag{6.42e}$$

A computer program was used to determine the pulse widths and to evaluate the performance of modified SPWM. The harmonic profile is shown in Figure 6.19 for five pulses per half-cycle. The number of pulses q in the 60° period is normally related to the frequency ratio, particularly in three-phase inverters, by

$$\frac{f_c}{f_o} = 6q + 3 \tag{6.43}$$

The instantaneous output voltage is $v_o = V_s(g_1 - g_4)$. The algorithm for generating the gating signals is similar to that for sinusoidal PWM in Section 6.6.3, except the reference signal is a sine wave from 60° to 120° only.

6.6.5 Phase-Displacement Control

Voltage control can be obtained by using multiple inverters and summing the output voltages of individual inverters. A single-phase full-bridge inverter in Figure 6.2a can be perceived as the sum of two half-bridge inverters in Figure 6.1a. A 180°-phase

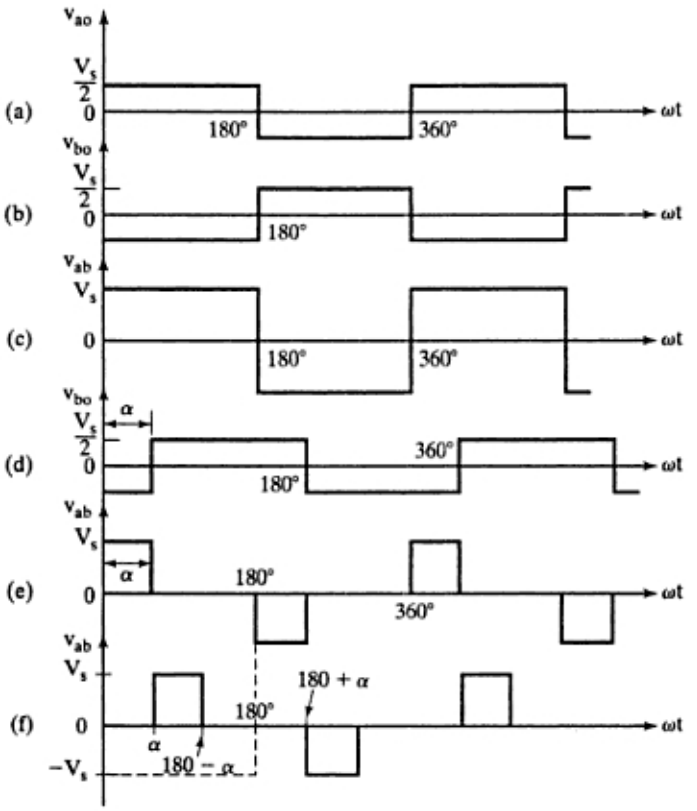


FIGURE 6.20

Phase-displacement control.

displacement produces an output voltage as shown in Figure 6.20c, whereas a delay (or displacement) angle of α produces an output as shown in Figure 6.20e.

For example, the gate signal g_1 for the half-bridge inverter can be delayed by angle α to produce the gate signal g_2.

The rms output voltage,

$$V_o = V_s\sqrt{\frac{\alpha}{\pi}} \tag{6.44}$$

If

$$V_{ao} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2V_s}{n\pi} \sin n\omega t$$

then

$$v_{bo} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2V_s}{n\pi} \sin n(\omega t - \alpha)$$

The instantaneous output voltage,

$$v_{ab} = v_{ao} - v_{bo} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2V_s}{n\pi} [\sin n\omega t - \sin n(\omega t - \alpha)]$$

which, after using $\sin A - \sin B = 2 \sin[(A - B)/2] \cos[(A + B)/2]$, can be simplified to

$$v_{ab} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_s}{n\pi} \sin \frac{n\alpha}{2} \cos n\left(\omega t - \frac{\alpha}{2}\right) \tag{6.45}$$

The rms value of the fundamental output voltage is

$$V_{o1} = \frac{4V_s}{\sqrt{2}} \sin \frac{\alpha}{2} \tag{6.46}$$

Equation (6.46) indicates that the output voltage can be varied by changing the delay angle. This type of control is especially useful for high-power applications, requiring a large number of switching devices in parallel.

If the gate signals g_1 and g_2 are delayed by angles $\alpha_1 = \alpha$ and $\alpha_2 (= \pi - \alpha)$, the output voltage v_{ab} has a quarter-wave symmetry at $\pi/2$ as shown in Figure 6.20f. Thus, we get

$$v_{ao} = \sum_{n=1}^{\infty} \frac{2V_s}{n\pi} \sin(n(\omega t - \alpha)) \qquad \text{for } n = 1, 3, 5, \ldots$$

$$v_{bo} = \sum_{n=1}^{\infty} \frac{2V_s}{n\pi} \sin[n(\omega t - \pi + \alpha)] \qquad \text{for } n = 1, 3, 5, \ldots$$

$$v_{ab} = v_{ao} - v_{bo} = \sum_{n=1}^{\infty} \frac{4V_s}{n\pi} \cos(n\alpha) \sin(n\omega t) \qquad \text{for } n = 1, 3, 5 \tag{6.47}$$

6.7 ADVANCED MODULATION TECHNIQUES

The SPWM, which is most commonly used, suffers from drawbacks (e.g., low fundamental output voltage). The other techniques that offer improved performances are:

Trapezoidal modulation
Staircase modulation
Stepped modulation
Harmonic injection modulation
Delta modulation

For the sake of simplicity, we shall show the output voltage v_{ao}, for a half-bridge inverter in Figure 6.1a. For a full-bridge inverter, $v_o = v_{ao} - v_{bo}$, where v_{bo} is the inverse of v_{ao}.

Trapezoidal modulation. The gating signals are generated by comparing a triangular carrier wave with a modulating trapezoidal wave [3] as shown in Figure 6.21.

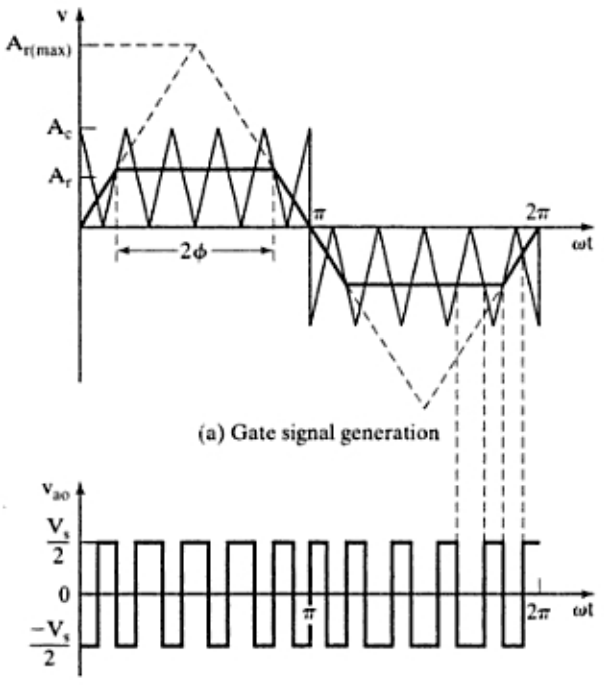


FIGURE 6.21
Trapezoidal modulation.

The trapezoidal wave can be obtained from a triangular wave by limiting its magnitude to $\pm A_r$, which is related to the peak value $A_{r(\max)}$ by

$$A_r = \sigma A_{r(\max)}$$

where σ is called the *triangular factor*, because the waveform becomes a triangular wave when $\sigma = 1$. The modulation index M is

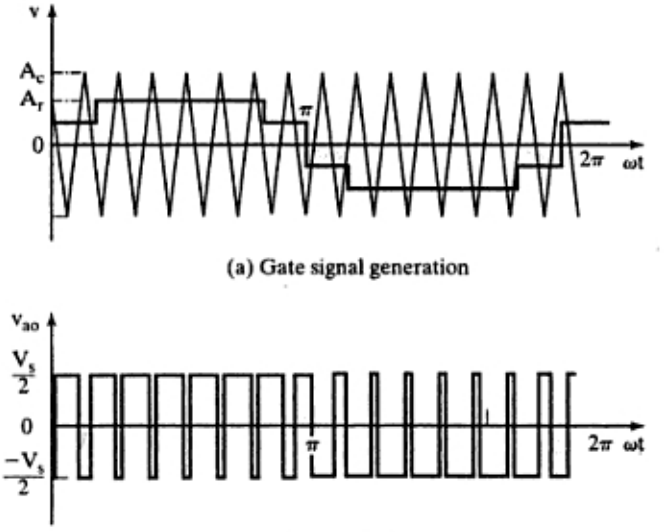
$$M = \frac{A_r}{A_c} = \frac{\sigma A_{r(\max)}}{A_c} \quad \text{for } 0 \leq M \leq 1 \tag{6.48}$$

The angle of the flat portion of the trapezoidal wave is given by

$$2\phi = (1 - \sigma)\pi \tag{6.49}$$

For fixed values of $A_{r(\max)}$ and A_c, M that varies with the output voltage can be varied by changing the triangular factor σ. This type of modulation increases the peak fundamental output voltage up to $1.05V_s$, but the output contains LOHs.

Staircase modulation. The modulating signal is a staircase wave, as shown in Figure 6.22. The staircase is not a sampled approximation to the sine wave. The levels of the stairs are calculated to eliminate specific harmonics. The modulation frequency



(a) Gate signal generation

(b) Output voltage

FIGURE 6.22
Staircase modulation.

ratio m_f and the number of steps are chosen to obtain the desired quality of output voltage. This is an optimized PWM and is not recommended for fewer than 15 pulses in one cycle. It has been shown [4] that for high fundamental output voltage and low DF, the optimum number of pulses in one cycle is 15 for two levels, 21 for three levels, and 27 for four levels. This type of control provides a high-quality output voltage with a fundamental value of up to $0.94V_s$.

Stepped modulation. The modulating signal is a stepped wave [4, 5] as shown in Figure 6.23. The stepped wave is not a sampled approximation to the sine wave. It is divided into specified intervals, say 20°, with each interval controlled individually to control the magnitude of the fundamental component and to eliminate specific harmonics. This type of control gives low distortion, but a higher fundamental amplitude compared with that of normal PWM control.

Harmonic injected modulation. The modulating signal is generated by injecting selected harmonics to the sine wave. This results in flat-topped waveform and reduces the amount of overmodulation. It provides a higher fundamental amplitude and low distortion of the output voltage. The modulating signal [6, 7] is generally composed of

$$v_r = 1.15 \sin \omega t + 0.27 \sin 3\omega t - 0.029 \sin 9\omega t \tag{6.50}$$

The modulating signal with third and ninth harmonic injections is shown in Figure 6.24. It should be noted that the injection of $3n$th harmonics does not affect the quality of the output voltage, because the output of a three-phase inverter does not contain triplen harmonics. If only the third harmonic is injected, v_r is given by

$$v_r = 1.15 \sin \omega t + 0.19 \sin 3\omega t \tag{6.51}$$

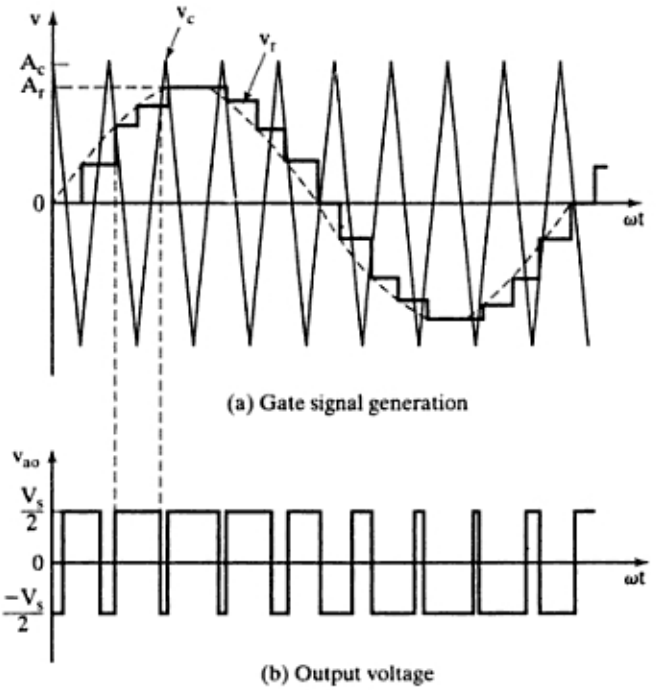


FIGURE 6.23
Stepped modulation.

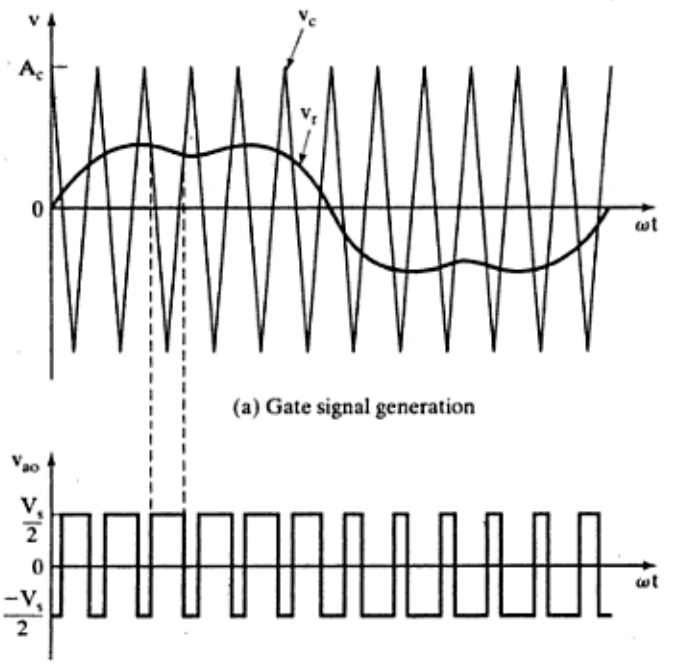


FIGURE 6.24
Selected harmonic injection modulation.

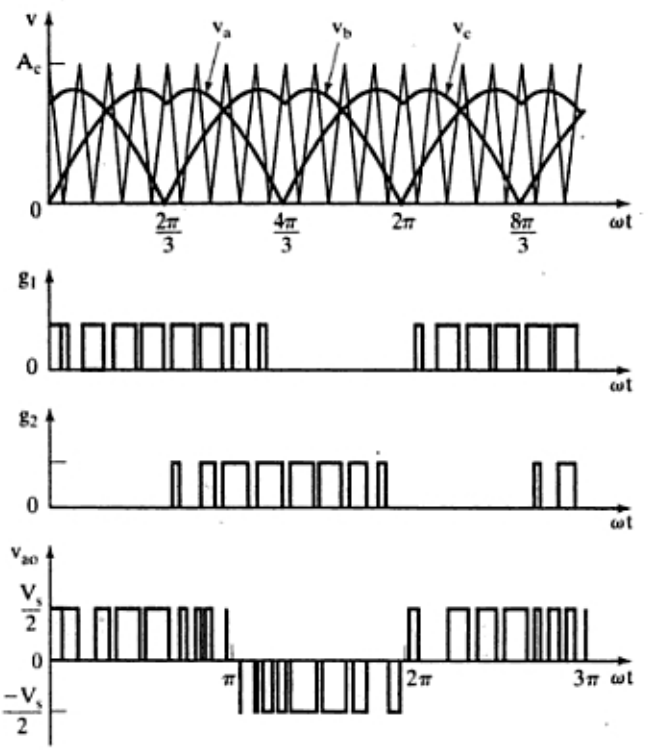


FIGURE 6.25
Harmonic injection modulation.

The modulating signal [8] can be generated from $2\pi/3$ segments of a sine wave as shown in Figure 6.25. This is the same as injecting $3n$th harmonics to a sine wave. The line-to-line voltage is sinusoidal PWM and the amplitude of the fundamental component is approximately 15% more than that of a normal sinusoidal PWM. Because each arm is switched off for one-third of the period, the heating of the switching devices is reduced.

Delta modulation. In delta modulation [9], a triangular wave is allowed to oscillate within a defined window ΔV above and below the reference sine wave v_r. The inverter switching function, which is identical to the output voltage v_o is generated from the vertices of the triangular wave v_c as shown in Figure 6.26. It is also known as *hysteresis modulation*. If the frequency of the modulating wave is changed keeping the slope of the triangular wave constant, the number of pulses and pulses widths of the modulated wave would change.

The fundamental output voltage can be up to $1V_s$ and is dependent on the peak amplitude A_r and frequency f_r of the reference voltage. The delta modulation can control the ratio of voltage to frequency, which is a desirable feature, especially in ac motor control.

6.8 VOLTAGE CONTROL OF THREE-PHASE INVERTERS

A three-phase inverter may be considered as three single-phase inverters and the output of each single-phase inverter is shifted by 120°. The voltage control techniques

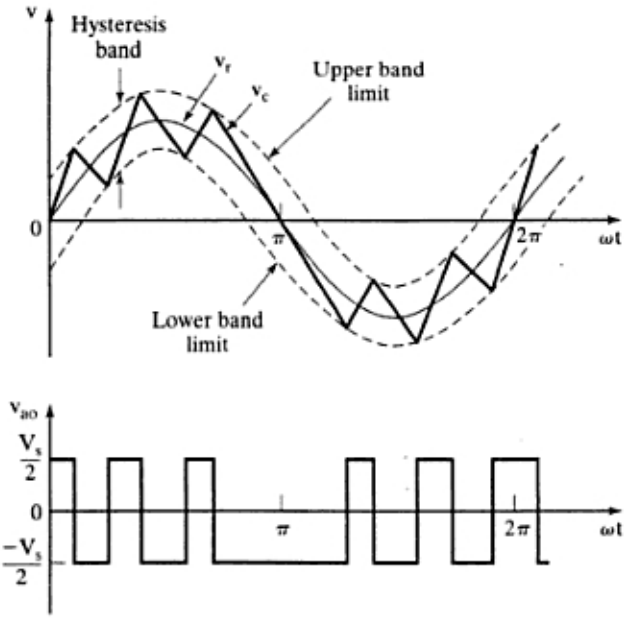


FIGURE 6.26
Delta modulation.

discussed in Section 6.6 are applicable to three-phase inverters. However, the following techniques are most commonly used for three-phase inverters.

Sinusoidal PWM
Third-harmonic PWM
60° PWM
Space vector modulation

6.8.1 Sinusoidal PWM

The generations of gating signals with sinusoidal PWM are shown in Figure 6.27a. There are three sinusoidal reference waves (v_{r_a}, v_{r_b}, and v_{r_c}) each shifted by 120°. A carrier wave is compared with the reference signal corresponding to a phase to generate the gating signals for that phase [10]. Comparing the carrier signal v_{cr} with the reference phases v_{ra}, v_{rb}, and v_{rc} produces g_1, g_3, and g_5, respectively, as shown in Figure 6.27b. The instantaneous line-to-line output voltage is $v_{ab} = V_s(g_1 - g_3)$. The output voltage as shown in Figure 6.27c, is generated by eliminating the condition that two switching devices in the same arm cannot conduct at the same time.

The normalized carrier frequency m_f should be odd multiple of three. Thus, all phase-voltage (v_{aN}, v_{bN}, and v_{cN}) are identical, but 120° out of phase without even harmonics; moreover, harmonics at frequencies multiple of three are identical in

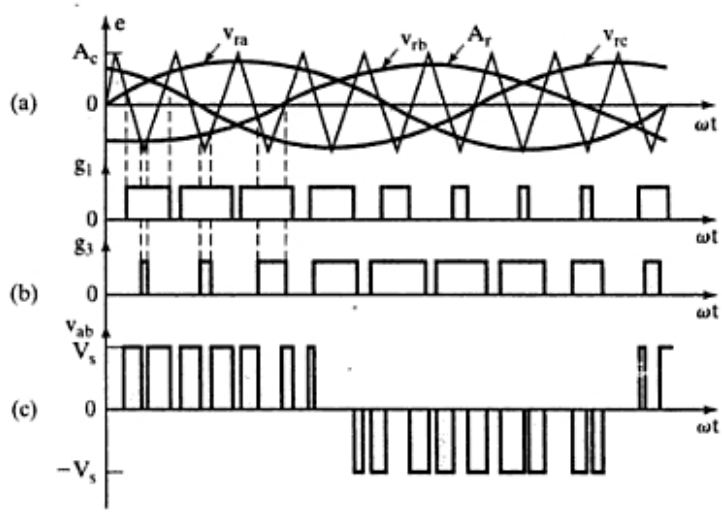


FIGURE 6.27

Sinusoidal pulse-width modulation for three-phase inverter.

amplitude and phase in all phases. For instance, if the ninth harmonic voltage in phase *a* is

$$v_{aN9}(t) = \hat{v}_9 \sin(9\omega t) \tag{6.52}$$

the corresponding ninth harmonic in phase *b* will be,

$$v_{bN9}(t) = \hat{v}_9 \sin(9(\omega t - 120°)) = \hat{v}_9 \sin(9\omega t - 1080°)) = \hat{v}_9 \sin(9\omega t) \tag{6.53}$$

Thus, the ac output line voltage $v_{ab} = v_{aN} - v_{bN}$ does not contain the ninth harmonic. Therefore, for odd multiples of three times the normalized carrier frequency m_f, the harmonics in the ac output voltage appear at normalized frequencies f_h centered around m_f and its multiples, specifically, at

$$n = jm_f \pm k \tag{6.54}$$

where $j = 1, 3, 5, \ldots$ for $k = 2, 4, 6, \ldots$; and $j = 2, 4, \ldots$ for $k = 1, 5, 7, \ldots$, such that n is not a multiple of three. Therefore, the harmonics are at $m_f \pm 2, m_f \pm 4 \ldots$, $2m_f \pm 1, 2m_f \pm 5, \ldots, 3m_f \pm 2, 3m_f \pm 4, \ldots, 4m_f \pm 1, 4m_f \pm 5, \ldots$. For nearly sinusoidal ac load current, the harmonics in the dc link current are at frequencies given by

$$n = jm_f \pm k \pm 1 \tag{6.55}$$

CHAPTER 9

Multilevel Inverters

The learning objectives of this chapter are as follows:

- To learn the switching technique for multilevel inverters and their types
- To study the operation and features of multilevel inverters
- To understand the advantages and disadvantages of multilevel inverters
- To learn about the control strategy to address capacitor voltage unbalancing
- To learn the potential applications of multilevel inverters

9.1 INTRODUCTION

The voltage source inverters produce an output voltage or a current with levels either 0 or $\pm V_{dc}$. They are known as the two-level inverter. To obtain a quality output voltage or a current waveform with a minimum amount of ripple content, they require high-switching frequency along with various pulse-width modulation (PWM) strategies. In high-power and high-voltage applications, these two-level inverters, however, have some limitations in operating at high frequency mainly due to switching losses and constraints of device ratings. Moreover, the semiconductor switching devices should be used in such a manner as to avoid problems associated with their series–parallel combinations that are necessary to obtain capability of handling high voltages and currents.

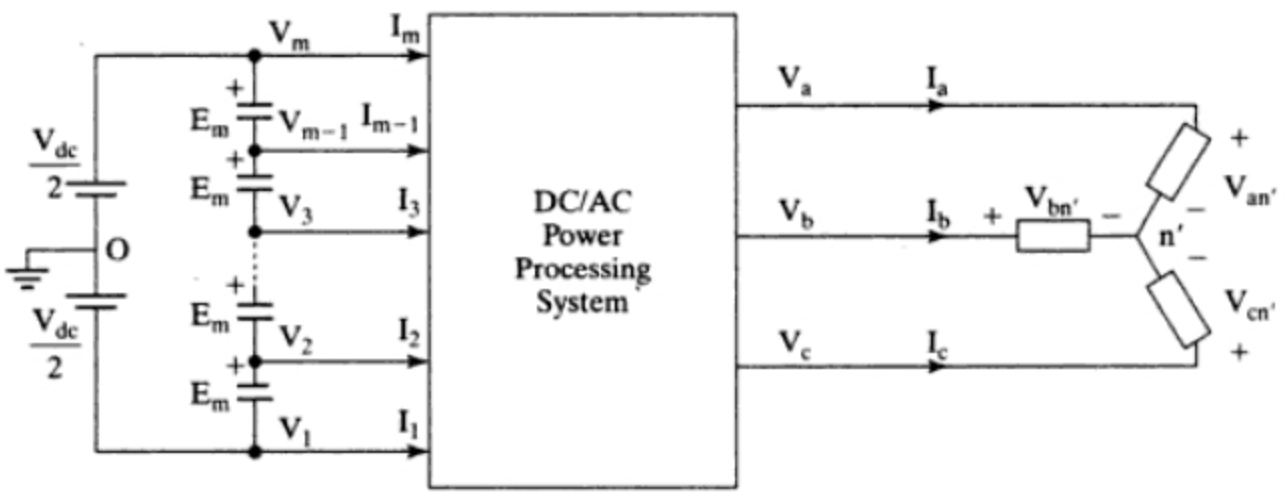
The multilevel inverters have drawn tremendous interest in the power industry. They present a new set of features that are well suited for use in reactive power compensation. It may be easier to produce a high-power, high-voltage inverter with the multilevel structure because of the way in which device voltage stresses are controlled in the structure. Increasing the number of voltage levels in the inverter without requiring higher ratings on individual devices can increase the power rating. The unique structure of multilevel voltage source inverters' allows them to reach high voltages with low harmonics without the use of transformers or series-connected synchronized-switching devices. As the number of voltage levels increases, the harmonic content of the output voltage waveform decreases significantly [1, 2].

9.2 MULTILEVEL CONCEPT

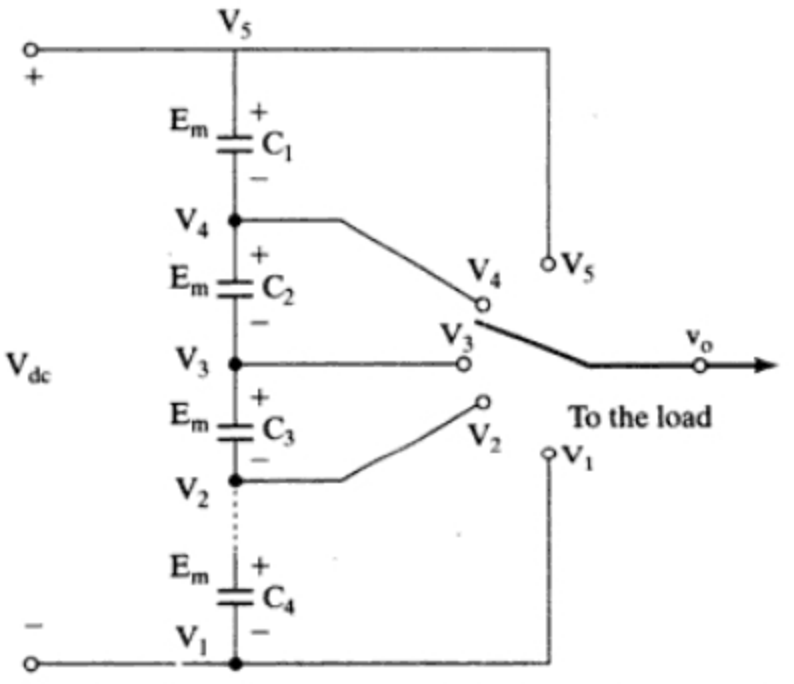
Let us consider a three-phase inverter system [4], as shown in Figure 9.1a, with a dc voltage V_{dc}. Series-connected capacitors constitute the energy tank for the inverter, providing some nodes to which the multilevel inverter can be connected. Each capacitor has the same voltage E_m, which is given by

$$E_m = \frac{V_{dc}}{m-1} \tag{9.1}$$

where m denotes the number of levels. The term *level* is referred to as the number of nodes to which the inverter can be accessible. An m-level inverter needs $(m-1)$ capacitors.



(a) Three-phase multilevel power processing system



(b) Schematic of single pole of multilevel inverter by a switch

FIGURE 9.1

General topology of multilevel inverters.

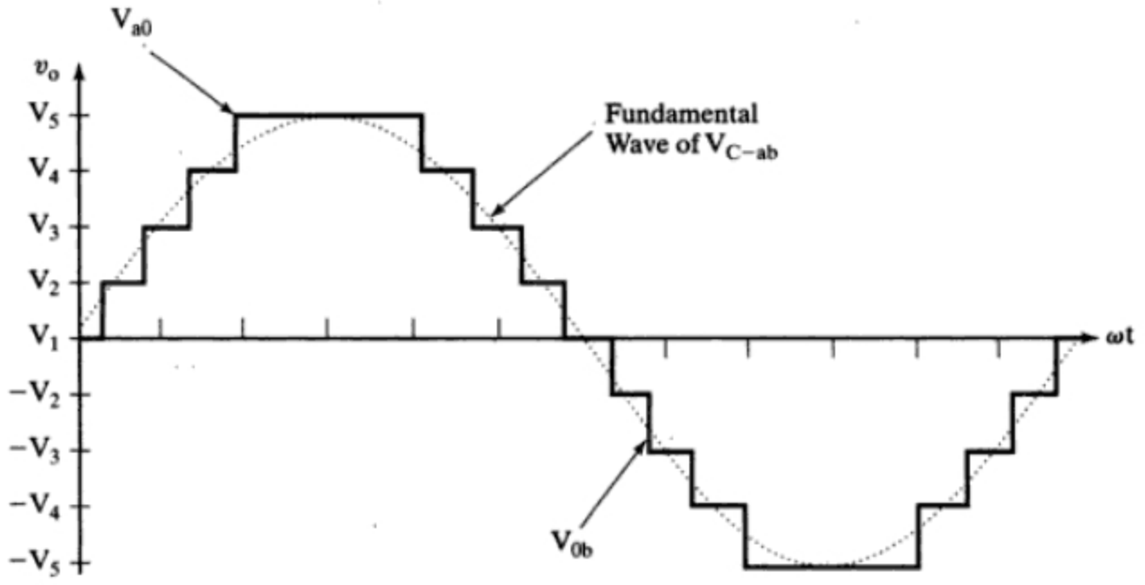


FIGURE 9.2

Typical output voltage of a five-level multilevel inverter.

Output phase voltages can be defined as voltages across output terminals of the inverter and the ground point denoted by o as shown in Figure 9.1a. Moreover, input node voltages and currents can be referred to input terminal voltages of the inverter with reference to ground point and the corresponding currents from each node of the capacitors to the inverter, respectively. For example, input node (dc) voltages are designated by V_1, V_2, etc. and the input node (dc) currents by I_1, I_2, etc., as shown in Figure 9.1a. V_a, V_b, and V_c, are the root-mean-square (rms) values of the line load voltages; I_a, I_b, and I_c are the rms values of the line load currents. Figure 9.1b shows the schematic of a pole in a multilevel inverter where v_a indicates an output phase voltage that can assume any voltage level depending on the selection of node (dc) voltage V_1, V_2, etc. Thus, a pole in a multilevel inverter can be regarded as a single-pole, multiple-throw switch. By connecting the switch to one node at a time, one can obtain the desired output. Figure 9.2 shows the typical output voltage of a five-level inverter.

The actual realization of the switch requires bidirectional switching devices for each node. The topological structure of multilevel inverter must (1) have less switching devices as far as possible, (2) be capable of withstanding very high input voltage for high-power applications, and (3) have lower switching frequency for each switching device.

9.3 TYPES OF MULTILEVEL INVERTERS

The general structure of the multilevel converter is to synthesize a near sinusoidal voltage from several levels of dc voltages, typically obtained from capacitor voltage sources. As the number of levels increases, the synthesized output waveform has more steps, which produce a staircase wave that approaches a desired waveform. Also, as more steps are added to the waveform, the harmonic distortion of the output wave decreases, approaching zero as the number of levels increases. As the number of levels increases, the voltage that can be spanned by summing multiple voltage levels also

increases. The output voltage during the positive half-cycle can be found from

$$v_{ao} = \sum_{n=1}^{m} E_n SF_n \tag{9.2}$$

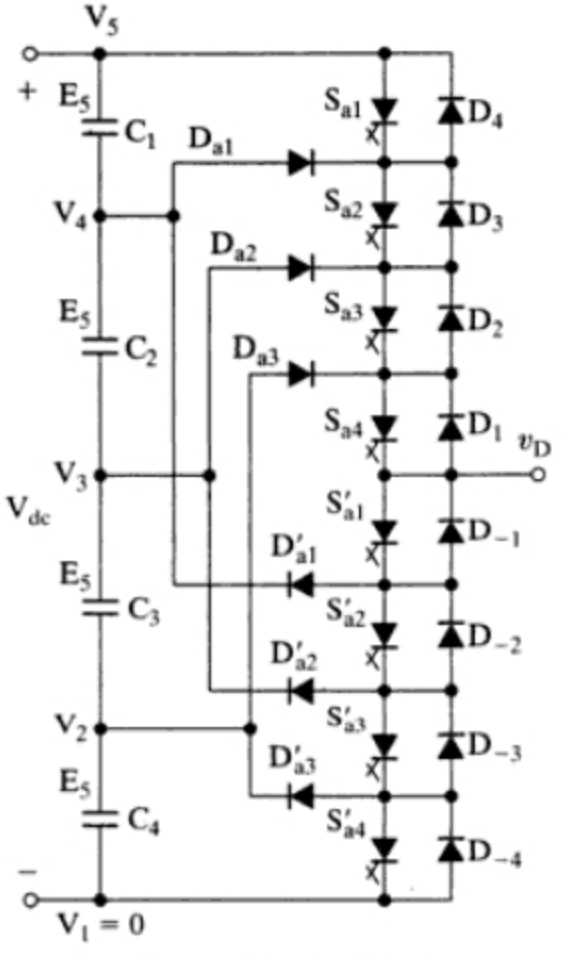
where SF_n is the switching or control function of nth node and it takes a value of 0 or 1. Generally, the capacitor terminal voltages E_1, E_2, ... all have the same value E_m. Thus, the peak output voltage is $v_{ao(\text{peak})} = (m-1)E_m = V_{dc}$. To generate an output voltage with both positive and negative values, the circuit topology has another switch to produce the negative part v_{ob} so that $v_{ab} = v_{ao} + v_{ob} = v_{ao} - v_{bo}$.

The multilevel inverters can be classified into three types [5].

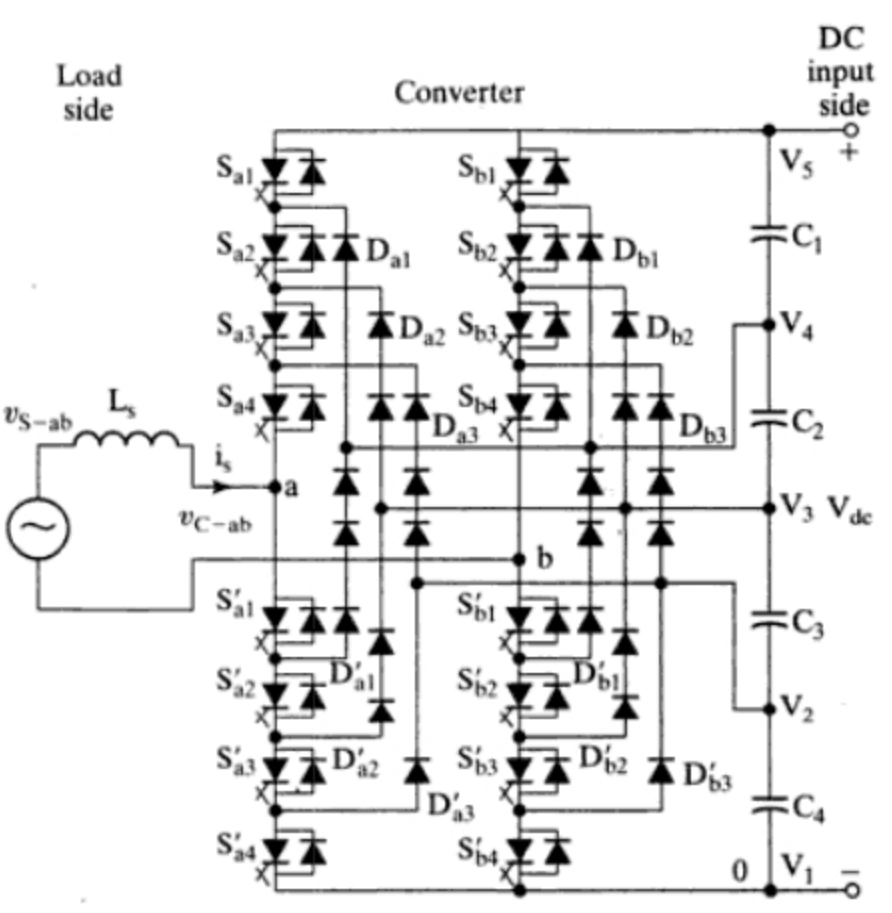
Diode-clamped multilevel inverter;
Flying-capacitors multilevel inverter;
Cascade multilevel inverter.

9.4 DIODE-CLAMPED MULTILEVEL INVERTER

A diode-clamped multilevel (m-level) inverter (DCMLI) typically consists of $(m-1)$ capacitors on the dc bus and produces m levels on the phase voltage. Figure 9.3a shows



(a) One leg of a bridge



(b) Single-phase bridge

FIGURE 9.3
Diode-clamped five-level bridge multilevel inverter. [Ref. 4]

one leg and Figure 9.3b shows a full-bridge five-level diode-clamped converter. The numbering order of the switches is S_{a1}, S_{a2}, S_{a3}, S_{a4}, S'_{a1}, S'_{a2}, S'_{a3}, and S'_{a4}. The dc bus consists of four capacitors, C_1, C_2, C_3, and C_4. For a dc bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress is limited to one capacitor voltage level $V_{dc}/4$ through clamping diodes. An m-level inverter leg requires $(m-1)$ capacitors, $2(m-1)$ switching devices and $(m-1)(m-2)$ clamping diodes.

9.4.1 Principle of Operation

To produce a staircase-output voltage, let us consider only one leg of the five-level inverter, as shown in Figure 9.3a, as an example. A single-phase bridge with two legs is shown in Figure 9.3b. The *dc rail* 0 is the reference point of the output phase voltage. The steps to synthesize the five-level voltages are as follows:

1. For an output voltage level $v_{ao} = V_{dc}$, turn on all upper-half switches S_{a1} through S_{a4}.
2. For an output voltage level $v_{ao} = 3V_{dc}/4$, turn on three upper switches S_{a2} through S_{a4} and one lower switch S'_{a1}.
3. For an output voltage level $v_{ao} = V_{dc}/2$, turn on two upper switches S_{a3} through S_{a4} and two lower switches S'_{a1} and S'_{a2}.
4. For an output voltage level $v_{ao} = V_{dc}/4$, turn on one upper switch S_{a4} and three lower switches S'_{a1} through S'_{a3}.
5. For an output voltage level $v_{ao} = 0$, turn on all lower half switches S'_{a1} through S'_{a4}.

Table 9.1 shows the voltage levels and their corresponding switch states. State condition 1 means the switch is on, and state 0 means the switch is off. It should be noticed that each switch is turned on only once per cycle and there are four complementary switch pairs in each phase. These pairs for one leg of the inverter are (S_{a1}, S'_{a1}), (S_{a2}, S'_{a2}), (S_{a3}, S'_{a3}), and (S_{a4}, S'_{a4}). Thus, if one of the complementary switch pairs is turned on, the other of the same pair must be off. Four switches are always turned on at the same time.

Figure 9.4 shows the phase voltage waveform of the five-level inverter. The line voltage consists of the positive phase-leg voltage of terminal a and the negative phase-leg voltage of terminal b. Each phase-leg voltage tracks one-half of the sinusoidal wave. The

TABLE 9.1 Diode-Clamped Voltage Levels and Their Switch States

Output V_{a0}	Switch State							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S'_{a1}	S'_{a2}	S'_{a3}	S'_{a4}
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0
$V_4 = 3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_3 = V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2 = V_{dc}/4$	0	0	0	1	1	1	1	0
$V_1 = 0$	0	0	0	0	1	1	1	1

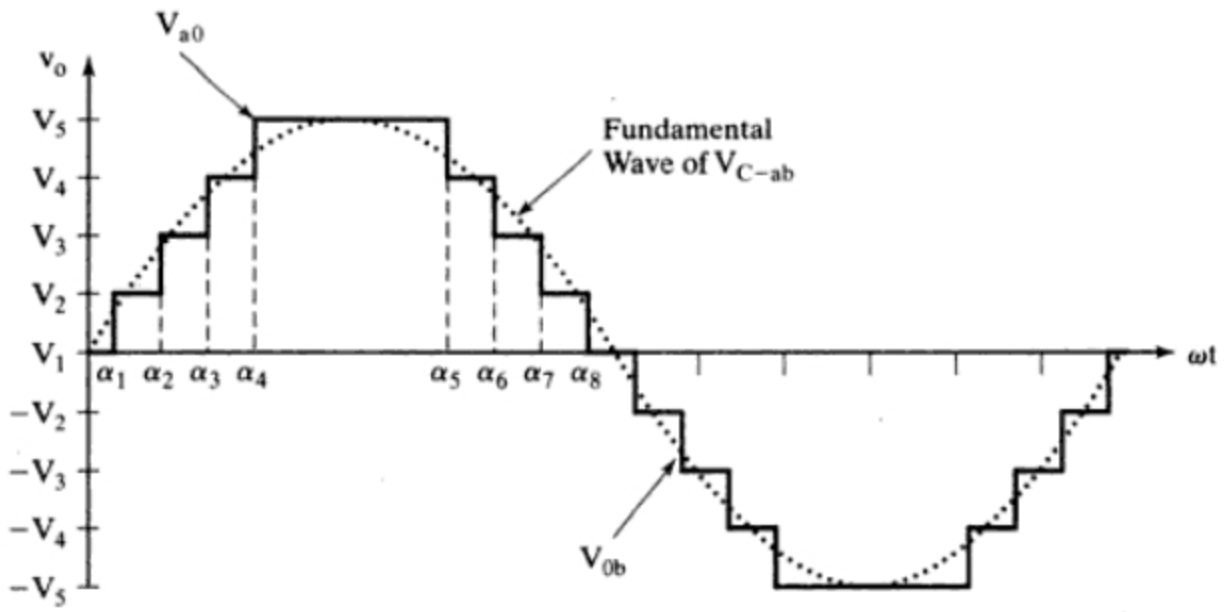


FIGURE 9.4

Phase and fundamental voltage waveforms of a five-level inverter.

resulting line voltage is a nine-level staircase wave. This implies that an m-level converter has an m-level output phase-leg voltage and a $(2m - 1)$-level output line voltage.

9.4.2 Features of Diode-Clamped Inverter

The main features are as follows:

1. *High-voltage rating for blocking diodes*: Although each switching device is only required to block a voltage level of $V_{dc}/(m - 1)$, the clamping diodes need to have different reverse voltage blocking ratings. For example, when all lower devices S'_{a1} through S'_{a4} are turned on, diode D'_{a1} needs to block three capacitor voltages, or $3V_{dc}/4$. Similarly, diodes D_{a2} and D'_{a2} need to block $2V_{dc}/4$, and D_{a3} needs to block $V_{dc}/4$. Even though each main switch is supposed to block the nominal blocking voltage, the blocking voltage of each clamping diode in the diode clamping inverter is dependent on its position in the structure. In an m-level leg, there can be two diodes, each seeing a blocking voltage of

$$V_D = \frac{m - 1 - k}{m - 1} V_{dc} \tag{9.3}$$

where m is the number of levels;
k goes from 1 to $(m - 2)$;
V_{dc} is the total dc link voltage.

If the blocking voltage rating of each diode is the same as that of the switching device, the number of diodes required for each phase is $N_D = (m - 1) \times (m - 2)$. This number represents a quadratic increase in m. Thus, for $m = 5$, $N_D = (5 - 1) \times (5 - 2) = 12$. When m is sufficiently high, the number of diodes makes the system impractical to implement, which in effect limits the number of levels.

2. *Unequal switching device rating*: We can notice from Table 9.1 that switch S_{a1} conducts only during $v_{ao} = V_{dc}$, whereas switch S_{a4} conducts over the entire cycle except during the interval when $v_{ao} = 0$. Such an unequal conduction duty requires different current ratings for the switching devices. Therefore, if the inverter design uses the average duty cycle to find the device ratings, the upper switches may be oversized, and the lower switches may be undersized. If the design uses the worst-case condition, then each phase has $2 \times (m - 2)$ upper devices oversized.
3. *Capacitor voltage unbalance*: Because the voltage levels at the capacitor terminals are different, the currents supplied by the capacitors are also different. When operating at unity power factor, the discharging time for inverter operation (or charging time for rectifier operation) for each capacitor is different. Such a capacitor charging profile repeats every half-cycle, and the result is unbalanced capacitor voltages between different levels. This voltage unbalance problem in a multilevel converter can be resolved by using approaches such as replacing capacitors by a controlled constant dc voltage source, PWM voltage regulators, or batteries.

The major advantages of the diode-clamped inverter can be summarized as follows:

- When the number of levels is high enough, the harmonic content is low enough to avoid the need for filters.
- Inverter efficiency is high because all devices are switched at the fundamental frequency.
- The control method is simple.

The major disadvantages of the diode-clamped inverter can be summarized as follows:

- Excessive clamping diodes are required when the number of levels is high.
- It is difficult to control the real power flow of the individual converter in multiconverter systems.

9.4.3 Improved Diode-Clamped Inverter

The problem of multiple blocking voltages of the clamping diodes can be addressed by connecting an appropriate number of diodes in series, as shown in Figure 9.5. However, due to mismatches of the diode characteristics, the voltage sharing is not equal. An improved version of the diode-clamped inverter [6] is shown in Figure 9.6 for five levels. The numbering order of the switches is S_1, S_2, S_3, S_4, S'_1, S'_2, S'_3, and S'_4. There are a total of eight switches and 12 diodes of equal voltage rating, which are the same as the diode-clamping inverter with series-connected diodes. This pyramid architecture is extensible to any level, unless otherwise practically limited. A five-level inverter leg requires $(m - 1 =)$ 4 capacitors, $(2(m - 1) =)$ 8 switches and $((m - 1)(m - 2) =)$ 12 clamping diodes.

Principle of operation. The modified diode-clamped inverter can be decomposed into two-level switching cells. For an m-level inverter, there are $(m - 1)$ switching cells. Thus, for $m = 5$, there are 4 cells: In cell 1, S_2, S_3, and S_4 are always on whereas S_1 and S'_1 are switched alternatively to produce an output voltage $V_{dc}/2$ and

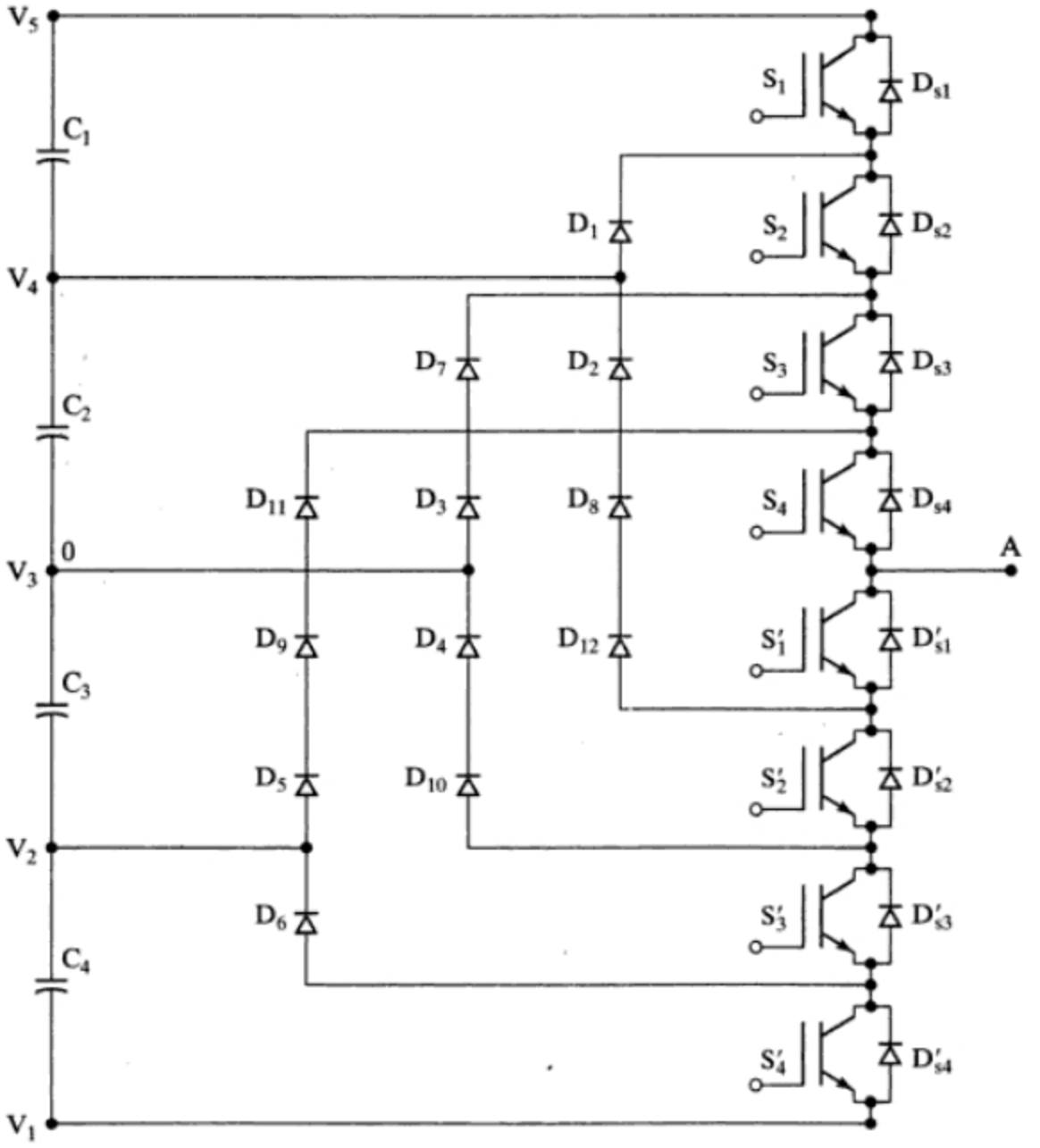


FIGURE 9.5

Diode-clamped multilevel inverter with diodes in series. [Ref. 6]

$V_{dc}/4$, respectively. Similarly, in cell 2, S_3, S_4, and S'_1 are always on whereas S_2 and S'_2 are switched alternatively to produce an output voltage $V_{dc}/4$ and 0, respectively. In cell 3, S_4, S'_1, and S'_2 are always on whereas S_3 and S'_3 are switched alternatively to produce an output voltage 0 and $-V_{dc}/2$, respectively. In final cell 4, S'_1, S'_2, and S'_3 are always on whereas S_4 and S'_4 are switched alternatively to produce an output voltage $-V_{dc}/4$ and $-V_{dc}/2$, respectively.

Each switching cell works actually as a normal two-level inverter, except that each forward or freewheeling path in the cell involves $(m - 1)$ devices instead of only one. Taking cell 2 as an example, the forward path of the up-arm involves D_1, S_2, S_2, and S_4, whereas the freewheeling path of the up-arm involves S'_1, D_{12}, D_8, and D_2, connecting the inverter output to $V_{dc}/4$ level for either positive or negative current flow. The forward path of the down-arm involves S'_1, S'_2, D_{10}, and D_4, whereas the freewheeling path of the down-arm involves D_3, D_7, S_3, and S_4, connecting the inverter output to

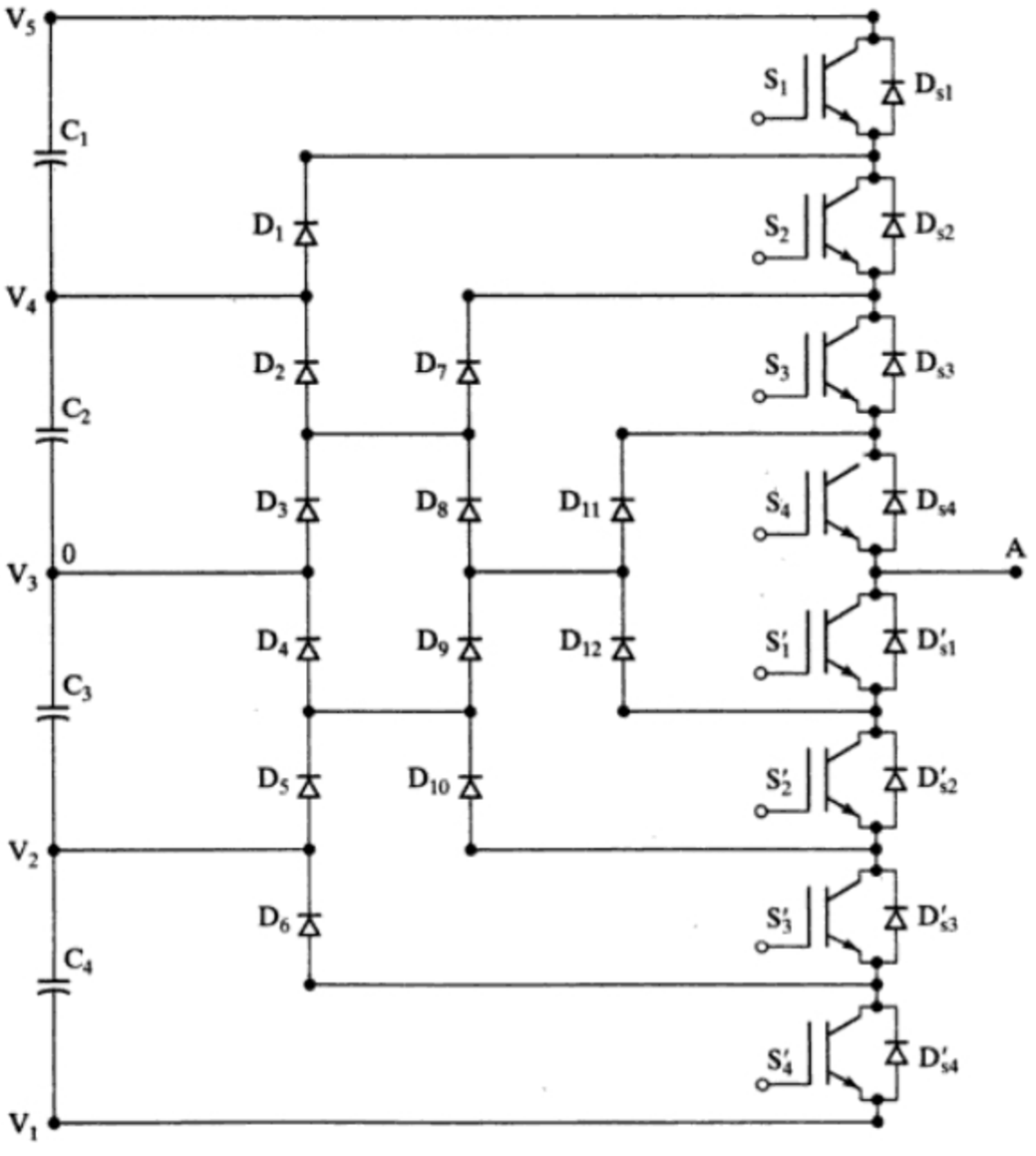


FIGURE 9.6

Modified diode-clamed inverter with distributed clamping diodes. [Ref. 6]

zero level for either positive or negative current flow. The following rules govern the switching of an m-level inverter:

1. At any moment, there must be $(m - 1)$ neighboring switches that are on.
2. For each two neighboring switches, the outer switch can only be turned on when the inner switch is on.
3. For each two neighboring switches, the inner switch can only be turned off when the outer switch is off.

9.5 FLYING-CAPACITORS MULTILEVEL INVERTER

Figure 9.7 shows a single-phase, full-bridge, five-level converter based on a flying-capacitors multilevel inverter (FCMLI) [5]. The numbering order of the switches is

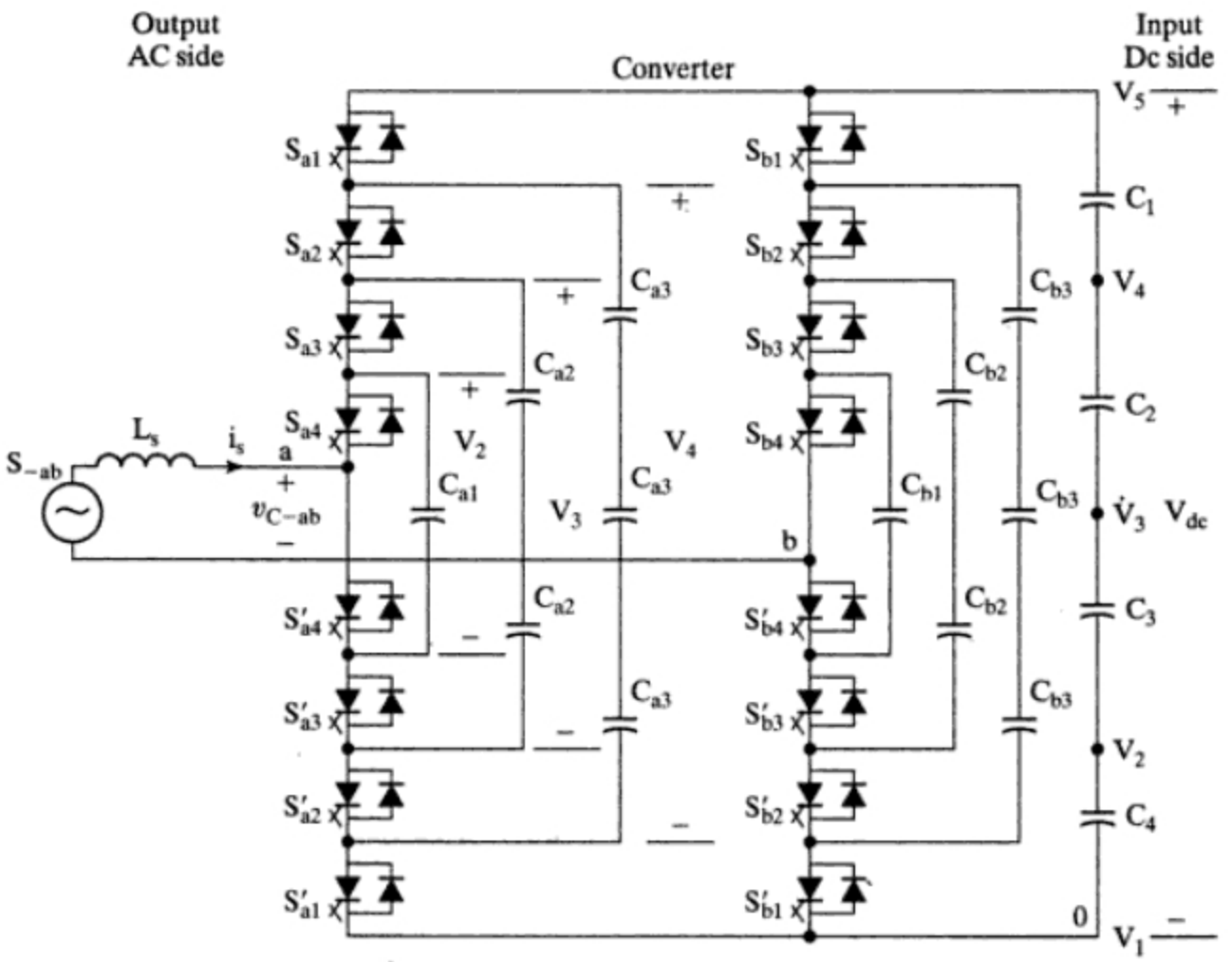


FIGURE 9.7

Circuit diagram of a five-level, flying-capacitors, single-phase inverter. [Ref. 5]

S_{a1}, S_{a2}, S_{a3}, S_{a4}, S'_{a4}, S'_{a3}, S'_{a2}, and S'_{a1}. Note that the order is numbered differently from that of the diode-clamped inverter in Figure 9.3. The numbering is immaterial as along as the switches are turned on and off in the right sequence to produce the desired output waveform. Each phase leg has an identical structure. Assuming that each capacitor has the same voltage rating, the series connection of the capacitors indicates the voltage level between the clamping points. Three inner-loop balancing capacitors (C_{a1}, C_{a2}, and C_{a3}) for phase-leg a are independent from those for phase-leg b. All phase legs share the same dc-link capacitors, C_1 through C_4.

The voltage level for the flying-capacitors converter is similar to that of the diode-clamped type of converter. That is, the phase voltage v_{ao} of an m-level converter has m levels (including the reference level), and the line voltage v_{ab} has $(2m - 1)$ levels. Assuming that each capacitor has the same voltage rating as the switching device, the dc bus needs $(m - 1)$ capacitors for an m-level converter. The number of capacitors required for each phase is $N_C = \sum_{j=1}^{m}(m - j)$. Thus, for $m = 5$, $N_C = 10$.

9.5.1 Principle of Operation

To produce a staircase-output voltage, let us consider the one leg of the five-level inverter shown in Figure 9.7 as an example. The dc rail 0 is the reference point of

the output phase voltage. The steps to synthesize the five-level voltages are as follows:

1. For an output voltage level $v_{ao} = V_{dc}$, turn on all upper-half switches S_{a1} through S_{a4}.
2. For an output voltage level $v_{ao} = 3V_{dc}/4$, there are four combinations:
   a. $v_{ao} = V_{dc} - V_{dc}/4$ by turning on devices S_{a1}, S_{a2}, S_{a3}, and S'_{a4}.
   b. $v_{ao} = 3V_{dc}/4$ by turning on devices S_{a2}, S_{a3}, S_{a4}, and S'_{a1}.
   c. $v_{ao} = V_{dc} - 3V_{dc}/4 + V_{dc}/2$ by turning on devices S_{a1}, S_{a3}, S_{a4}, and S'_{a2}.
   d. $v_{ao} = V_{dc} - V_{dc}/2 + V_{dc}/4$ by turning on devices S_{a1}, S_{a2}, S_{a4}, and S'_{a3}.
3. For an output voltage level $v_{ao} = V_{dc}/2$, there are six combinations:
   a. $v_{ao} = V_{dc} - V_{dc}/2$ by turning on devices S_{a1}, S_{a2}, S'_{a3}, and S'_{a4}.
   b. $v_{ao} = V_{dc}/2$ by turning on devices S_{a3}, S_{a4}, S'_{a1}, and S'_{a2}.
   c. $v_{ao} = V_{dc} - 3V_{dc}/4 + V_{dc}/2 - V_{dc}/4$ by turning on devices S_{a1}, S_{a3}, S'_{a2}, and S'_{a4}.
   d. $v_{ao} = V_{dc} - 3V_{dc}/4 + V_{dc}/4$ by turning on devices S_{a1}, S_{a4}, S'_{a2}, and S'_{a3}.
   e. $v_{ao} = 3V_{dc}/4 - V_{dc}/2 + V_{dc}/4$ by turning on devices S_{a2}, S_{a4}, S'_{a1}, and S'_{a3}.
   f. $v_{ao} = 3V_{dc}/4 - V_{dc}/4$ by turning on devices S_{a2}, S_{a3}, S'_{a1}, and S'_{a4}.
4. For an output voltage level $v_{ao} = V_{dc}/4$, there are four combinations:
   a. $v_{ao} = V_{dc} - 3V_{dc}/4$ by turning on devices S_{a1}, S'_{a2}, S'_{a3}, and S'_{a4}.
   b. $v_{ao} = V_{dc}/4$ by turning on devices S_{a4}, S'_{a1}, S'_{a2}, and S'_{a3}.
   c. $v_{ao} = V_{dc}/2 - V_{dc}/4$ by turning on devices S_{a3}, S'_{a1}, S'_{a2}, and S'_{a4}.
   d. $v_{ao} = 3V_{dc}/4 - V_{dc}/2$ by turning on devices S_{a2}, S'_{a1}, S'_{a3}, and S'_{a4}.
5. For an output voltage level $v_{ao} = 0$, turn on all lower half switches S'_{a1} through S'_{a4}.

There are many possible switch combinations to generate the five-level output voltage. Table 9.2, however, lists a possible combination of the voltage levels and their corresponding switch states. Using such a switch combination requires each device to be switched only once per cycle. It can be noticed from Table 9.2 that the switching devices have unequal turn-on time. Like the diode-clamped inverter, the line voltage consists of the positive phase-leg voltage of terminal *a* and the negative phase-leg voltage of terminal *b*. The resulting line voltage is a nine-level staircase wave. This implies that an m-level converter has an m-level output phase-leg voltage and a $(2m - 1)$-level output line voltage.

TABLE 9.2 One Possible Switch Combination of the Flying-Capacitors Inverter

Output	Switch State							
V_{a0}	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S'_{a4}	S'_{a3}	S'_{a2}	S'_{a1}
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0
$V_4 = 3V_{dc}/4$	1	1	1	0	1	0	0	0
$V_3 = V_{dc}/2$	1	1	0	0	1	1	0	0
$V_2 = V_{dc}/4$	1	0	0	0	1	1	1	0
$V_1 = 0$	0	0	0	0	1	1	1	1

9.5.2 Features of Flying-Capacitors Inverter

The main features are as follows:

1. *Large number of capacitors*: The inverter requires a large number of storage capacitors. Assuming that the voltage rating of each capacitor is the same as that of a switching device, an m-level converter requires a total of $(m-1) \times (m-2)/2$ auxiliary capacitors per phase leg in addition to $(m-1)$ main dc bus capacitors. On the contrary, an m-level diode-clamp inverter only requires $(m-1)$ capacitors of the same voltage rating. Thus, for $m = 5$, $N_C = 4 \times 3/2 + 4 = 10$ compared with $N_C = 4$ for the diode-clamped type.
2. *Balancing capacitor voltages*: Unlike the diode-clamped inverter, the FCMLI has redundancy at its inner voltage levels. A voltage level is redundant if two or more valid switch combinations can synthesize it. The availability of voltage redundancies allows controlling the individual capacitor voltages. In producing the same output voltage, the inverter can involve different combinations of capacitors allowing preferential charging or discharging of individual capacitors. This flexibility makes it easier to manipulate the capacitor voltages and keep them at their proper values. It is possible to employ two or more switch combinations for middle voltage levels (i.e., $3V_{dc}/4$, $V_{dc}/2$, and $V_{dc}/4$) in one or several output cycle to balance the charging and discharging of the capacitors. Thus, by proper selection of switch combinations, the flying-capacitors multilevel converter may be used in real power conversions. However, when it involves real power conversions, the selection of a switch combination becomes very complicated, and the switching frequency needs to be higher than the fundamental frequency.

The major advantages of the flying-capacitors inverter can be summarized as follows:

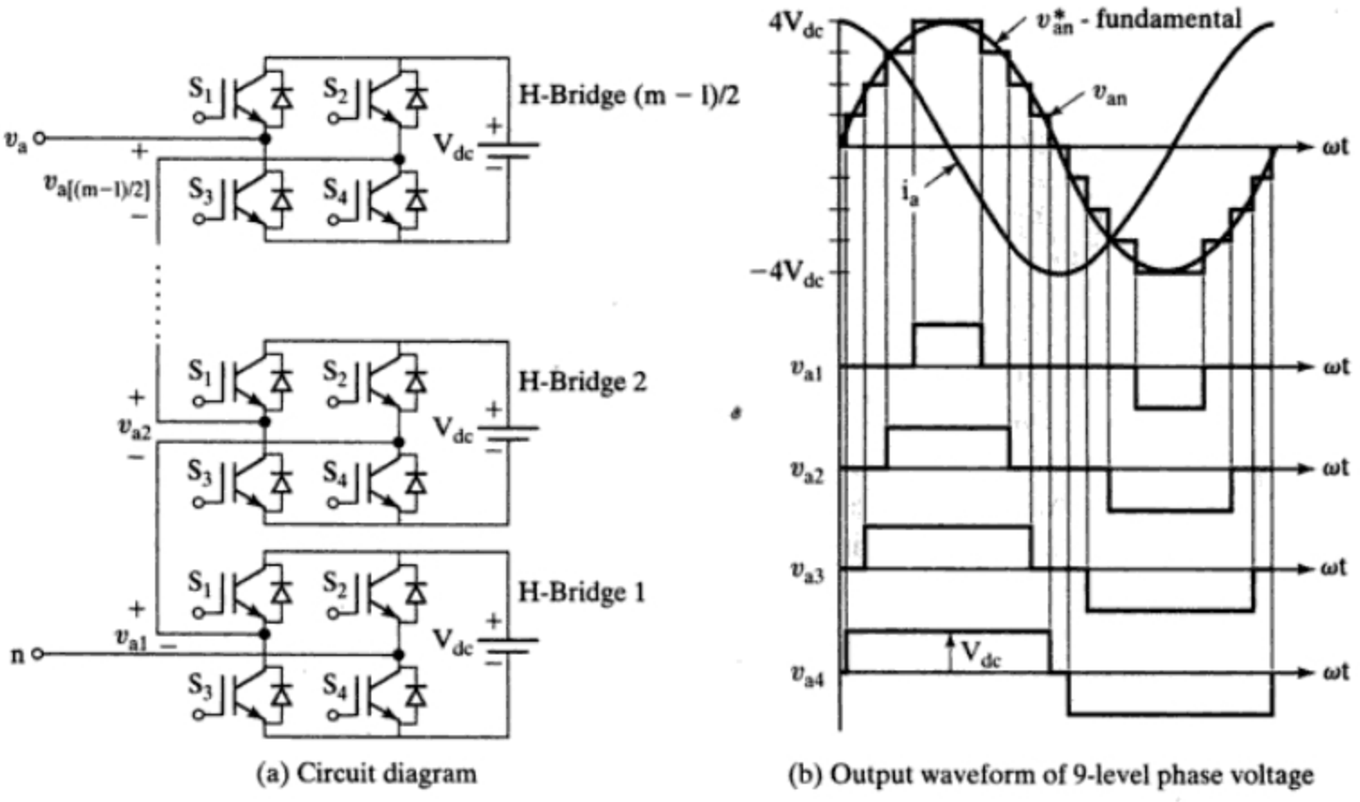
- Large amounts of storage capacitors can provide capabilities during power outages.
- These inverters provide switch combination redundancy for balancing different voltage levels.
- Like the diode-clamp inverter with more levels, the harmonic content is low enough to avoid the need for filters.
- Both real and reactive power flow can be controlled.

The major disadvantages of the flying-capacitors inverter can be summarized as follows:

- An excessive number of storage capacitors is required when the number of levels is high. High-level inverters are more difficult to package with the bulky power capacitors and are more expensive too.
- The inverter control can be very complicated, and the switching frequency and switching losses are high for real power transmission.

9.6 CASCADED MULTILEVEL INVERTER

A cascaded multilevel inverter consists of a series of H-bridge (single-phase, full-bridge) inverter units. The general function of this multilevel inverter is to synthesize a



(a) Circuit diagram

(b) Output waveform of 9-level phase voltage

FIGURE 9.8

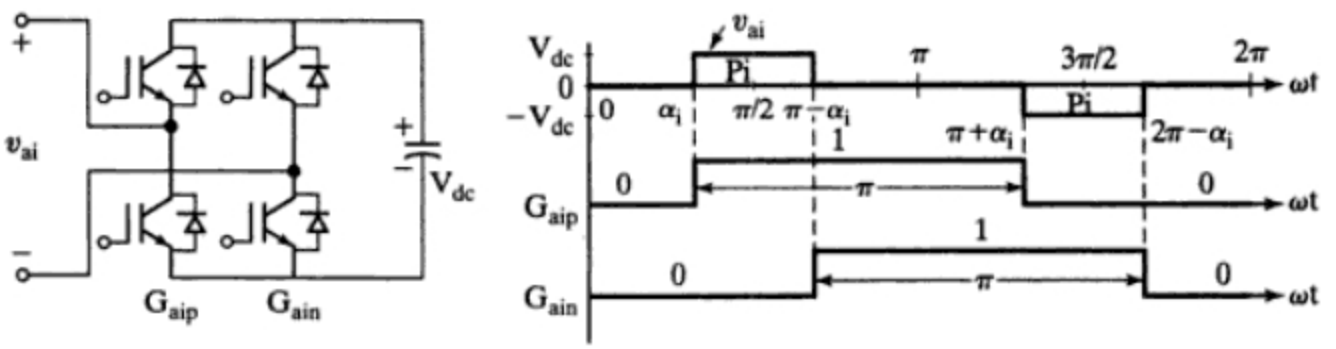
Single-phase multilevel cascaded H-bridge inverter. [Ref. 7]

desired voltage from several separate dc sources (SDCSs), which may be obtained from batteries, fuel cells, or solar cells. Figure 9.8a shows the basic structure of a single-phase cascaded inverter with SDCSs [7]. Each SDCS is connected to an H-bridge inverter. The ac terminal voltages of different level inverters are connected in series. Unlike the diode-clamp or flying-capacitors inverter, the cascaded inverter does not require any voltage-clamping diodes or voltage-balancing capacitors.

9.6.1 Principle of Operation

Figure 9.8b shows the synthesized phase voltage waveform of a five-level cascaded inverter with four SDCSs. The phase output voltage is synthesized by the sum of four inverter outputs, $v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4}$. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$, by connecting the dc source to the ac output side by different combinations of the four switches, S_1, S_2, S_3, and S_4. Using the top level as the example, turning on S_1 and S_4 yields $v_{a4} = +V_{dc}$. Turning on S_2 and S_3 yields $v_{a4} = -V_{dc}$. Turning off all switches yields $v_4 = 0$. Similarly, the ac output voltage at each level can be obtained in the same manner. If N_S is the number of dc sources, the output phase voltage level is $m = N_S + 1$. Thus, a five-level cascaded inverter needs four SDCSs and four full bridges. Controlling the conducting angles at different inverter levels can minimize the harmonic distortion of the output voltage.

The output voltage of the inverter is almost sinusoidal, and it has less than 5% total harmonic distribution (THD) with each of the H-bridges switching only at



(a) One H-bridge

(b) Switching time

FIGURE 9.9

Generation of quasi-square waveform. [Ref. 7]

fundamental frequency. If the phase current i_a, as shown in Figure 9.8b, is sinusoidal and leads or lags the phase voltage v_{an} by 90°, the average charge to each dc capacitor is equal to zero over one cycle. Therefore, all SDCS capacitor voltages can be balanced.

Each H-bridge unit generates a quasi-square waveform by phase shifting its positive and negative phase-leg-switching timings. Figure 9.9 shows the switching timings to generate a quasi-square waveform of an H-bridge. It should be noted that each switching device always conducts for 180° (or half-cycle), regardless of the pulse width of the quasi-square wave. This switching method makes all of the switching device current stresses equal.

9.6.2 Features of Cascaded Inverter

The main features are as follows:

- For real power conversions from ac to dc and then dc to ac, the cascaded inverters need separate dc sources. The structure of separate dc sources is well suited for various renewable energy sources such as fuel cell, photovoltaic, and biomass.
- Connecting dc sources between two converters in a back-to-back fashion is not possible because a short circuit can be introduced when two back-to-back converters are not switching synchronously.

The major advantages of the cascaded inverter can be summarized as follows:

- Compared with the diode-clamped and flying-capacitors inverters, it requires the least number of components to achieve the same number of voltage levels.
- Optimized circuit layout and packaging are possible because each level has the same structure and there are no extra clamping diodes or voltage-balancing capacitors.
- Soft-switching techniques can be used to reduce switching losses and device stresses.

The major disadvantage of the cascaded inverter are as follows:

- It needs separate dc sources for real power conversions, thereby limiting its applications.

Example 9.1 Finding Switching Angles to Eliminate Specific Harmonics

The phase voltage waveform for a cascaded inverter is shown in Figure 9.10 for $m = 6$ (including 0 level). (a) Find the generalized Fourier series of the phase voltage. (b) Find the switching angles to eliminate 5th, 7th, 11th, and 13th harmonics if the peak fundamental phase voltage is 80% of its maximum value. (c) Find the fundamental component B_1, THD, and the distortion factor (DF).

Solution

a. For a cascaded inverter with m levels (including 0) per half-phase, the output voltage per leg is

$$v_{an} = v_{a1} + v_{a2} + v_{a3} + \cdots + v_{am-1} \tag{9.4}$$

Due to the quarter-wave symmetry along the x-axis, both Fourier coefficients A_0 and A_n are zero. We get B_n as

$$B_n = \frac{4V_{dc}}{\pi}\left[\int_{\alpha_1}^{\pi/2} \sin(n\omega t)d(\omega t) + \int_{\alpha_2}^{\pi/2} \sin(n\omega t)d(\omega t) + \cdots + \int_{\alpha_m-1}^{\pi/2} \sin(n\omega t)d(\omega t)\right] \tag{9.5}$$

$$B_n = \frac{4V_{dc}}{n\pi}\left[\sum_{j=1}^{m-1} \cos(n\alpha_j)\right] \tag{9.6}$$

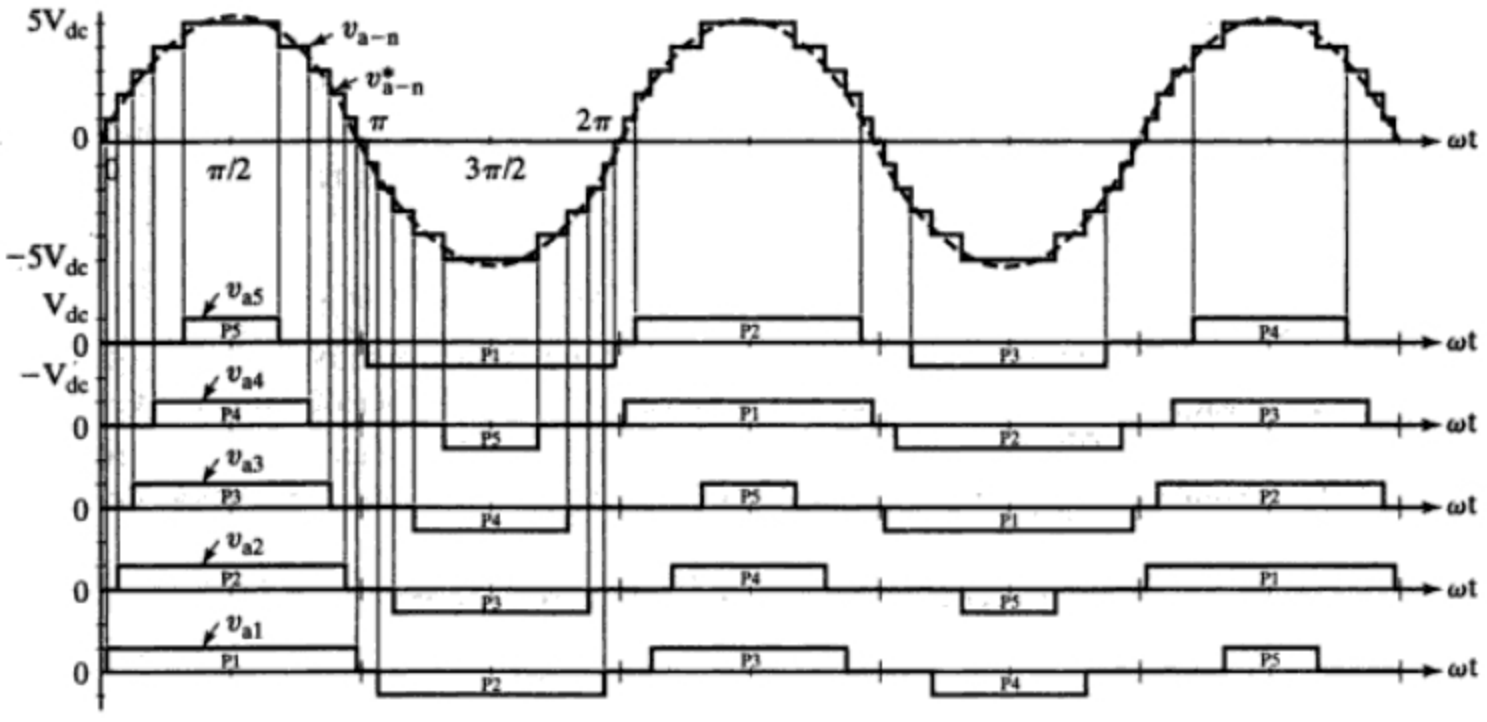


FIGURE 9.10

Switching pattern swapping of the cascade inverter for balancing battery charge. [Ref. 7]

which gives the instantaneous phase voltage v_{an} as

$$v_{an}(\omega t) = \frac{4V_{dc}}{n\pi}\left[\sum_{j=1}^{m-1}\cos(n\alpha_j)\right]\sin(n\omega t) \tag{9.7}$$

b. If the peak output phase voltage $V_{an(peak)}$ must equal to the carrier phase voltage, $V_{cr(peak)} = (m-1)V_{dc}$. Thus, the modulation index becomes

$$M = \frac{V_{cr(peak)}}{V_{an(peak)}} = \frac{V_{cr(peak)}}{(m-1)V_{dc}} \tag{9.8}$$

The conducting angles $\alpha_1, \alpha_2, \ldots, \alpha_{m-1}$ can be chosen such that the total harmonic distortion of the phase voltage is minimized. These angles are normally chosen so as to cancel some predominant lower frequency harmonics. Thus, to eliminate 5th, 7th, 11th, and 13th harmonics provided that the peak fundamental phase voltage is 80% of its maximum value, we must solve the following equations for modulation index $M = 0.8$.

$$\begin{aligned}
\cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) + \cos(5\alpha_4) + \cos(5\alpha_5) &= 0\\
\cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) + \cos(7\alpha_4) + \cos(7\alpha_5) &= 0\\
\cos(11\alpha_1) + \cos(11\alpha_2) + \cos(11\alpha_3) + \cos(11\alpha_4) + \cos(11\alpha_5) &= 0\\
\cos(13\alpha_1) + \cos(13\alpha_2) + \cos(13\alpha_3) + \cos(13\alpha_4) + \cos(13\alpha_5) &= 0\\
\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \cos(\alpha_4) + \cos(\alpha_5) &\\
= (m-1)M &\\
= 5 \times 0.8 = 4 &
\end{aligned} \tag{9.9}$$

This set of nonlinear transcendental equations can be solved by an iterative method such as the Newton–Raphson method. Using Mathcad, we get

$$\alpha_1 = 6.57°, \alpha_2 = 18.94°, \alpha_3 = 27.18°, \alpha_4 = 45.15°, \text{ and } \alpha_5 = 62.24°$$

Thus, if the inverter output is symmetrically switched during the positive half-cycle of the fundamental voltage to $+V_{dc}$ at 6.57°, $+2V_{dc}$ at 18.94°, $+3V_{dc}$ at 27.18°, $+4V_{dc}$ at 45.15°, and $+5V_{dc}$ at 62.24° and similarly in the negative half-cycle to $-V_{dc}$ at 186.57°, $-2V_{dc}$ at 198.94°, $-3V_{dc}$ at 207.18°, $-4V_{dc}$ at 225.15°, and $-5V_{dc}$ at 242.24°, the output voltage cannot contain the 5th, 7th, 11th, and 13th harmonics.

c. Using Mathcad, we get $B_1 = 5.093\%$, THD = 5.975%, and DF = 0.08%

Note: The duty cycle for each of the voltage levels is different. This means that the level-1 dc source discharges much sooner than the level-5 dc source. However, by using a switching pattern-swapping scheme among the various levels every half-cycle, as shown in Figure 9.10, all batteries can be equally used (discharged) or charged [7]. For example, if the first pulse sequence is $P_1, P_2, \ldots, P_5$, then the next sequence is P_2, P_3, P_4, P_5, P_1, and so on.

9.7 APPLICATIONS

There is considerable interest in applying voltage source inverters in high-power applications such as in utility systems for controlled sources of reactive power. In the steady-state operation, an inverter can produce a controlled reactive current and

operates as a static volt–ampere reactive (VAR)-compensator (STATCON). Also, these inverters can reduce the physical size of the compensator and improve its performance during power system contingencies. The use of a high-voltage inverter makes possible direct connection to the high-voltage (e.g., 13-kV) distribution system, eliminating the distribution transformer and reducing system cost. In addition, the harmonic content of the inverter waveform can be reduced with appropriate control techniques and thus the efficiency of the system can be improved. The most common applications of multilevel converters include (1) reactive power compensation, (2) back-to-back intertie, and (3) variable speed drives.

9.7.1 Reactive Power Compensation

An inverter converts a dc voltage to an ac voltage; with a phase shift of 180°, the inverter can be operated as a dc–ac converter, that is, a controlled rectifier. With a purely capacitive load, the inverter operating as a dc–ac converter can draw reactive current from the ac supply. Figure 9.11 shows the circuit diagram of a multilevel converter directly connected to a power system for reactive power compensation. The load side is connected to the ac supply and the dc side is open, not connected to any dc voltage. For the control of the reactive power flow, the inverter gate control is phase shifted by 180°. The dc side capacitors act as the load.

When a multilevel converter draws pure reactive power, the phase voltage and current are 90° apart, and the capacitor charge and discharge can be balanced. Such a converter, when serving for reactive power compensation, is called a static-VAR generator (SVG). All three multilevel converters can be used in reactive power compensation without having the voltage unbalance problem.

The relationship of the source voltage vector $\mathbf{V_S}$ and the converter voltage vector $\mathbf{V_C}$ is simply $\mathbf{V_S} = \mathbf{V_C} + j\mathbf{I_C}X_S$, where $\mathbf{I_C}$ is the converter current vector, and X_S is

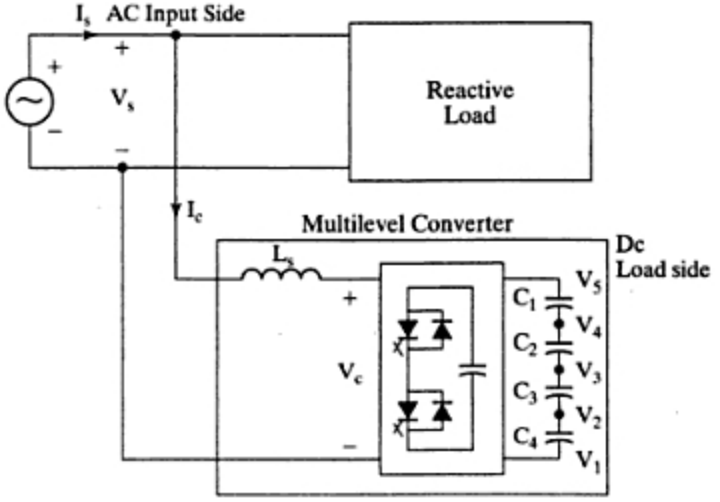


FIGURE 9.11

A multilevel converter connected to a power system for reactive power compensation. [Ref. 5]

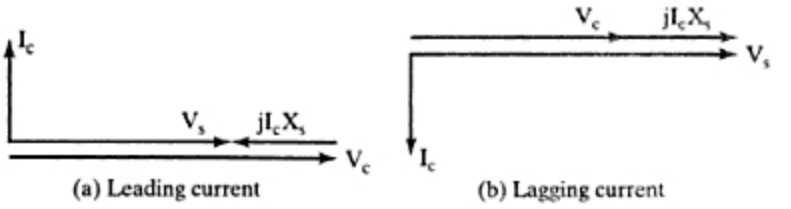


FIGURE 9.12

Phasor diagrams of the source and the converter voltages for reactive power compensation.

the reactance of the inductor L_S. Figure 9.12a illustrates that the converter voltage is in phase with the source voltage with a leading reactive current, whereas Figure 9.12b illustrates a lagging reactive current. The polarity and the magnitude of the reactive current are controlled by the magnitude of the converter voltage $\mathbf{V_C}$, which is a function of the dc bus voltage and the voltage modulation index, as expressed by Eqs. (9.7) and (9.8).

9.7.2 Back-to-Back Intertie

Figure 9.13 shows two diode-clamped multilevel converters that are interconnected with a dc capacitor link. The left-hand side converter serves as the rectifier for utility interface, and the right-hand side converter serves as the inverter to supply the ac load. Each switch remains on once per fundamental cycle. The voltage across each capacitor remains well balanced, while maintaining the staircase voltage wave, because the unbalance capacitor voltages on both sides tend to compensate each other. Such a dc capacitor link is categorized as the back-to-back intertie.

The back-to-back intertie that connects two asynchronous systems can be regarded as (1) a frequency changer, (2) a phase shifter, or (3) a power flow controller. The power flow between two systems can be controlled bidirectionally. Figure 9.14 shows the phasor diagram for real power transmission from the source end to the load end. This diagram indicates that the source current can be leading or lagging the source voltage. The converter voltage is phase shifted from the source voltage with a power angle, δ. If the source voltage is constant, then the current or power flow can be

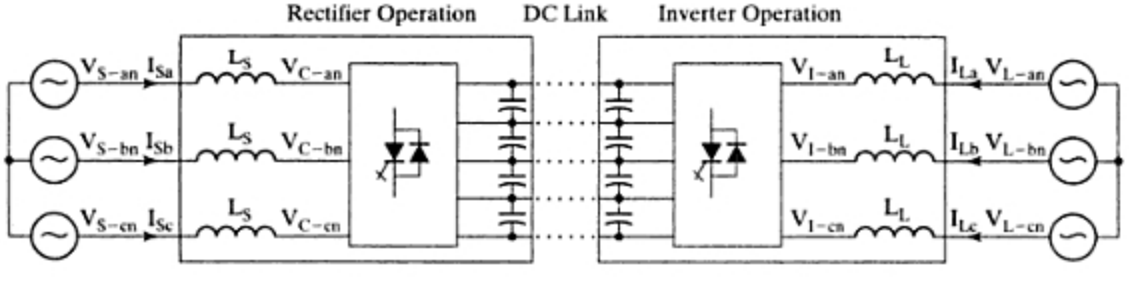
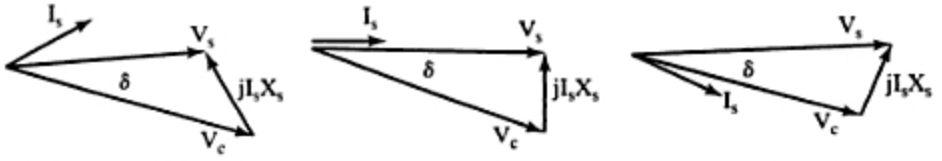


FIGURE 9.13

Back-to-back intertie system using two diode-clamped multilevel converters. [Ref. 5]



(a) Leading power factor (b) Unity power factor (c) Lagging power factor

FIGURE 9.14

Phasor diagram of the source voltage, converter voltage, and current showing real power conversions.

controlled by the converter voltage. For $\delta = 0$, the current is either 90° leading or lagging, meaning that only reactive power is generated.

9.7.3 Adjustable Speed Drives

The back-to-back intertie can be applied to a utility compatible adjustable speed drive (ASD) where the input is the constant frequency ac source from the utility supply and the output is the variable frequency ac load. For an ideal utility compatible system, it requires unity power factor, negligible harmonics, no electromagnetic interference (EMI), and high efficiency. The major differences, when using the same structure for ASDs and for back-to-back interties, are the control design and the size of the capacitor. Because the ASD needs to operate at different frequencies, the dc-link capacitor needs to be well sized to avoid a large voltage swing under dynamic conditions.

9.8 SWITCHING DEVICE CURRENTS

Let us take a three-level half-bridge inverter, as shown in Figure 9.15a, where V_o and I_0 indicate the rms load voltage and current, respectively. Assuming that the load inductance is sufficiently large and the capacitors maintain their voltages so that the output current is sinusoidal as given by

$$i_o = I_m \sin(\omega t - \phi) \tag{9.10}$$

where I_m is the peak value of the load current, and ϕ is the load impedance angle.

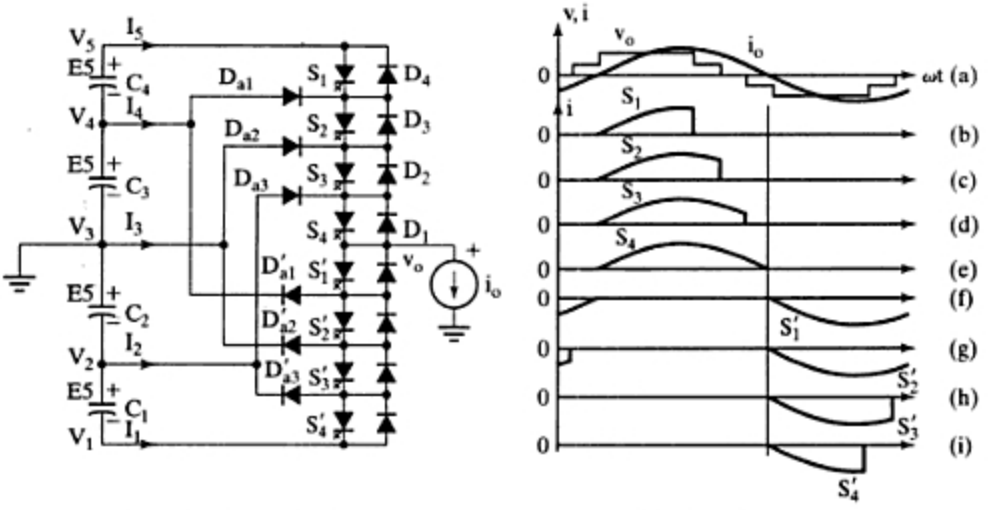
Figure 9.15b shows a typical current waveform of each switching device with a simple stepped control of output phase voltage. The most inner switches such as S_4 and S_1' carry more current than the most outer switches such as S_1 and S_4'.

Each input node current can be expressed as a function of the switching function SF_n as given by

$$i_n = SF_n i_o \qquad \text{for } n = 1, 2, \ldots, m \tag{9.11}$$

Because the single-pole multiple-throw switch multilevel inverter, shown in Figure 9.1b, is always connected to one and only one input node at every instant, the output load current could be drawn from one and only one input node. That is,

$$i_o = \sum_{n=1}^{m} i_n \tag{9.12}$$



(a) Five-level inverter circuit (b) Current waveforms

FIGURE 9.15

Half-bridge three-level diode-clamped inverter. [Ref. 4]

and the rms value of each current is expressed as

$$I_{o(\text{rms})}^2 = \sum_n^m I_{n(\text{rms})}^2 \tag{9.13}$$

where $I_{n(\text{rms})}$ is the rms current of the nth node given by

$$I_{n(\text{rms})} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} SF_n i_o^2 \, d(\omega t)} \qquad \text{for } n = 1, 2, \ldots, m \tag{9.14}$$

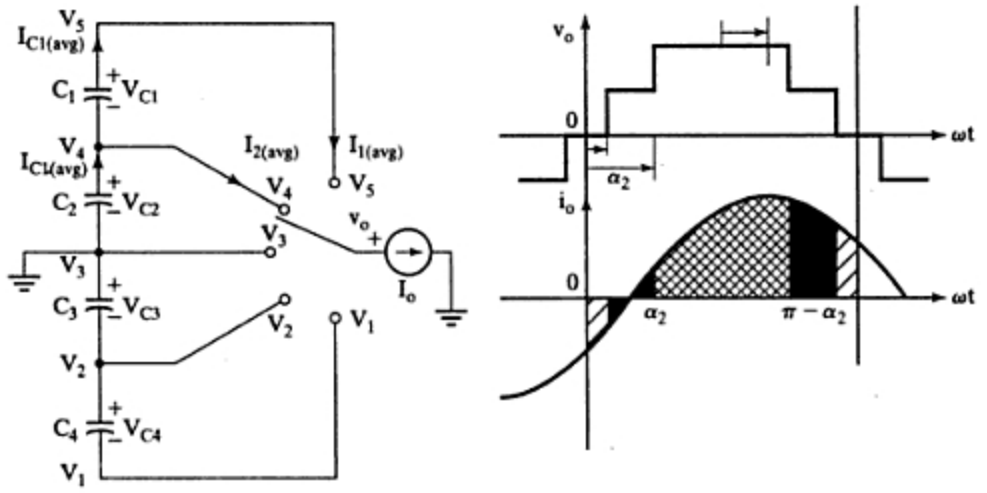
For balanced switching with respect to the ground level, we get

$$i_{1(\text{rms})}^2 = i_{5(\text{rms})}^2, \text{ and } i_{2(\text{rms})}^2 = i_{4(\text{rms})}^2 \tag{9.15}$$

It should be noted that by structure, the currents through the opposite switches such as $S'_1, \ldots, S'_4$ would have the same rms current through $S_4, \ldots, S_1$ respectively.

9.9 DC-LINK CAPACITOR VOLTAGE BALANCING

The voltage balancing of capacitors acting as an energy tank is very important for the multilevel inverter to work satisfactorily. Figure 9.16a shows the schematic of a half-bridge inverter with five levels and Figure 9.16b illustrates the stepped-output voltage and the sinusoidal load current $i_o = I_m \sin(\omega t - \phi)$..



(a) Schematic of a 3-level half-bridge inverter

(b) Distribution of load current

FIGURE 9.16

Charge distribution of capacitors. [Ref. 4]

The average value of the input node current i_1 is given by

$$I_{1(\text{avg})} = \frac{1}{2\pi}\int_{\alpha_2}^{\pi-\alpha_2} i_o d(\omega t) = \frac{1}{2\pi}\int_{\alpha_2}^{\pi-\alpha_2} I_m \sin(\omega t - \phi) d(\omega t)$$
$$= \frac{I_m}{\pi}\cos\phi\cos\alpha_2 \tag{9.16}$$

Similarly, the average value of the input node current i_2 is given by

$$I_{2(\text{avg})} = \frac{1}{2\pi}\int_{\alpha_1}^{\alpha_2} i_o d(\omega t) = \frac{1}{2\pi}\int_{\alpha_1}^{\alpha_2} I_m \sin(\omega t - \phi) d(\omega t)$$
$$= \frac{I_m}{\pi}\cos\phi(\cos\alpha_1 - \cos\alpha_2) \tag{9.17}$$

By symmetry, $I_{3(\text{avg})} = 0$, $I_{4(\text{avg})} = -I_{2(\text{avg})}$, and $I_{5(\text{avg})} = -I_{1(\text{avg})}$. Thus, each capacitor voltage should be regulated so that each capacitor supplies the average current per cycle as follows;

$$I_{C1(\text{avg})} = I_{1(\text{avg})} = \frac{I_m}{\pi}\cos\phi\cos\alpha_2 \tag{9.18}$$

$$I_{C2(\text{avg})} = I_{1(\text{avg})} + I_{2(\text{avg})} = \frac{I_m}{\pi}\cos\phi\cos\alpha_1 \tag{9.19}$$

Therefore, $I_{C1(avg)} < I_{C2(avg)}$ for $\alpha_1 < \alpha_2$. This results in the capacitor charge unbalancing, and more change flows from the inner capacitor C_2 (or C_3) than that of the outer capacitor C_1 (or C_4). Thus, each capacitor voltage should be regulated to supply the appropriate amount of average current; otherwise, its voltage V_{C2} (or V_{C3}) goes to the ground level as times goes. Equations (9.18) and (9.19) can be extended to the nth capacitor of a multilevel converter as given by

$$I_{Cn(avg)} = \frac{I_m}{\pi} \cos \phi \cos \alpha_n \tag{9.20}$$

Equations (9.18) and (9.19) give

$$\frac{\cos \alpha_2}{\cos \alpha_1} = \frac{I_{C2(avg)}}{I_{C1(avg)}} \tag{9.21}$$

which can be generalized for the nth and $(n-1)$th capacitors

$$\frac{\cos \alpha_n}{\cos \alpha_{n-1}} = \frac{I_{Cn(avg)}}{I_{C(n-1)(avg)}} \tag{9.22}$$

which means that the capacitor charge unbalancing exists regardless of the load condition and it depends on the control strategy such as $\alpha_1, \alpha_2, \ldots, \alpha_n$. Applying control strategy that forces the energy transfer from the outer capacitors to the inner capacitors can solve this unbalancing problem [9–11].

9.10 FEATURES OF MULTILEVEL INVERTERS

A multilevel inverter can eliminate the need for the step-up transformer and reduce the harmonics produced by the inverter. Although the multilevel inverter structure was initially introduced as a means of reducing the output waveform harmonic content, it was found [1] that the dc bus voltage could be increased beyond the voltage rating of an individual power device by the use of a voltage clamping network consisting of diodes. A multilevel structure with more than three levels can significantly reduce the harmonic content [2, 3]. By using voltage-clamping techniques, the system KV rating can be extended beyond the limits of an individual device. The intriguing feature of the multilevel inverter structures is their ability to scale up the kilovolt–ampere (kVA)-rating and also to improve the harmonic performance greatly without having to resort to PWM techniques. The key features of a multilevel structure follow:

- The output voltage and power increase with number of levels. Adding a voltage level involves adding a main switching device to each phase.
- The harmonic content decreases as the number of levels increases and filtering requirements are reduced.
- With additional voltage levels, the voltage waveform has more free-switching angles, which can be preselected for harmonic elimination.
- In the absence of any PWM techniques, the switching losses can be avoided. Increasing output voltage and power does not require an increase in rating of individual device.

TABLE 9.3 Comparisons of Component Requirements per Leg of Three Multilevel Converters [Ref. 5]

Converter Type	Diode Clamp	Flying Capacitors	Cascaded Inverters
Main switching devices	$(m-1)\times 2$	$(m-1)\times 2$	$(m-1)\times 2$
Main diodes	$(m-1)\times 2$	$(m-1)\times 2$	$(m-1)\times 2$
Clamping diodes	$(m-1)\times(m-2)$	0	0
Dc bus capacitors	$(m-1)$	$(m-1)$	$(m-1)/2$
Balancing capacitors	0	$(m-1)\times(m-2)/2$	0

- Static and dynamic voltage sharing among the switching devices is built into the structure through either clamping diodes or capacitors.
- The switching devices do not encounter any voltage-sharing problems. For this reason, multilevel inverters can easily be applied for high-power applications such as large motor drives and utility supplies.
- The fundamental output voltage of the inverter is set by the dc bus voltage V_{dc}, which can be controlled through a variable dc link.

9.11 COMPARISONS OF MULTILEVEL CONVERTERS

The multilevel converters [8] can replace the existing systems that use traditional multipulse converters without the need for transformers. For a three-phase system, the relationship between the number of levels m, and the number of pulses p, can be formulated by $p = 6 \times (m - 1)$. All three converters have the potential for applications in high-voltage, high-power systems such as an SVG without voltage unbalance problems because the SVG does not draw real power. The diode-clamped converter is most suitable for the back-to-back intertie system operating as a unified power flow controller. The other two types may also be suitable for the back-to-back intertie, but they would require more switching per cycle and more advanced control techniques to balance the voltage. The multilevel inverters can find potential applications in adjustable speed drives where the use of multilevel converters can not only solve harmonics and EMI problems but also avoid possible high-frequency switching dv/dt-induced motor failures.

Table 9.3 compares the component requirements per phase leg among the three multilevel converters. All devices are assumed to have the same voltage rating, but not necessarily the same current rating. The cascaded inverter uses a full bridge in each level as compared with the half-bridge version for the other two types. The cascaded inverter requires the least number of components and has the potential for utility interface applications because of its capabilities for applying modulation and soft-switching techniques.

SUMMARY

Multilevel converters can be applied to utility interface systems and motor drives. These converters offer a low output voltage THD, and a high efficiency and power

factor. There are three types of multilevel converters: (1) diode clamped, (2) flying capacitors, and (3) cascaded. The main advantages of multilevel converters include the following:

- They are suitable for high-voltage and high-current applications.
- They have higher efficiency because the devices can be switched at a low frequency.
- Power factor is close to unity for multilevel inverters used as rectifiers to convert ac to dc.
- No EMI problem exists.
- No charge unbalance problem results when the converters are in either charge mode (rectification) or drive mode (inversion).

The multilevel converters require balancing the voltage across the series-connected dc-bus capacitors. Capacitors tend to overcharge or completely discharge, at which condition the multilevel converter reverts to a three-level converter unless an explicit control is devised to balance the capacitor charge. The voltage-balancing technique must be applied to the capacitor during the operations of the rectifier and the inverter. Thus, the real power flow into a capacitor must be the same as the real power flow out of the capacitor, and the net charge on the capacitor over one cycle remains the same.

REFERENCES

[1] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," *IEEE Transactions on Industry Applications*, Vol. IA-17, No. 5, September/October 1981, pp. 518–523.

[2] P. M. Bhagwat and V. R. Stefanovic, "Generalized structure of a multilevel PWM inverter," *IEEE Transactions on Industry Applications*, Vol. 19, No. 6, November/December 1983, pp. 1057–1069.

[3] M. Carpita and S. Teconi, "A novel multilevel structure for voltage source inverter," *Proc. European Power Electronics*, 1991, pp. 90–94.

[4] N. S. Choi, L. G. Cho, and G. H. Cho, "A general circuit topology of multilevel inverter," *IEEE Power Electronics Specialist Conference*, 1991, pp. 96–103.

[5] J.-S. Lai, and F. Z. Peng, "Multilevel converters—a new breed of power converters," *IEEE Transactions on Industry Applications*, Vol. 32, No. 3, May/June 1996, pp. 509–517.

[6] X. Yuan and I. Barbi, "Fundamentals of a new diode clamping multilevel inverter," *IEEE Transactions on Power Electronics*, Vol. 15, No. 4, July 2000, pp. 711–718.

[7] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Transactions on Industry Applications*, Vol. 35, No. 1, January/February 1999, pp. 36–44.

[8] C. Hochgraf, R. I. Asseter, D. Divan, and T. A. Lipo, "Comparison of multilevel inverters for static-var compensation," IEEF-IAS Annual Meeting Record, 1994, pp. 921–928.

[9] L. M. Tolbert and T. G. Habetler, "Novel multilevel inverter carrier-based PWM method," *IEEE Transactions on Industry Applications*, Vol. 35, No. 5, September/October 1999, pp. 1098–1107.

[10] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel PWM methods at low modulation indices," *IEEE Transactions on Power Electronics*, Vol. 15, No. 4, July 2000, pp. 719–725.

[11] J. H. Seo, C. H. Choi, and D. S. Hyun, "A new simplified space—vector PWM method for three-level inverters," *IEEE Transactions on Power Electronics*, Vol. 16, No. 4, July 2001, pp. 545–550.

REVIEW QUESTIONS

9.1 What is a multilevel converter?
9.2 What is the basic concept of multilevel converters?
9.3 What are the features of a multilevel converter?
9.4 What are the types of multilevel converters?
9.5 What is a diode-clamped multilevel inverter?
9.6 What are the advantages of a diode-clamped multilevel inverter?
9.7 What are the disadvantages of a diode-clamped multilevel inverter?
9.8 What are the advantages of a modified diode-clamped multilevel inverter?
9.9 What is a flying-capacitors multilevel inverter?
9.10 What are the advantages of a flying-capacitors multilevel inverter?
9.11 What are the disadvantages of a flying-capacitors multilevel inverter?
9.12 What is a cascaded multilevel inverter?
9.13 What are the advantages of a cascaded multilevel inverter?
9.14 What are the disadvantages of a cascaded multilevel inverter?
9.15 What is a back-to-back intertie system?
9.16 What does the capacitor voltage unbalancing mean?
9.17 What are the possible applications of multilevel inverters?

PROBLEMS

9.1 A single-phase diode-clamped inverter has $m = 5$. Find the generalized Fourier series and THD of the phase voltage.
9.2 A single-phase diode-clamped inverter has $m = 5$. Find the peak voltage and current ratings of diodes and switching devices if $V_{dc} = 5$ kV and $i_o = 50 \sin(\theta - \pi/3)$.
9.3 A single-phase diode-clamped inverter has $m = 5$. Find **(a)** instantaneous, average and rms currents of each node, and **(b)** average and rms capacitor current if $V_{dc} = 5$ kV and $i_o = 50 \sin(\theta - \pi/3)$.
9.4 A single-phase flying-capacitors multilevel inverter has $m = 5$. Find the generalized Fourier series and THD of the phase voltage.
9.5 A single-phase flying-capacitors multilevel inverter has $m = 5$. Find the number of capacitors, the peak voltage and current ratings of diodes and switching devices if $V_{dc} = 5$ kV.
9.6 Compare the number of diodes and capacitors for diode clamp, flying capacitors and cascaded inverters if $m = 5$.
9.7 A single-phase cascaded multilevel inverter has $m = 5$. Find the peak voltage, and average and rms current ratings of H-bridge if $V_{dc} = 1$ kV and $i_o = 150 \sin(\theta - \pi/6)$.
9.8 A single-phase cascaded multilevel inverter has $m = 5$. Find the average current of each separate dc source (SDCS) if $V_{dc} = 1$ kV and $i_o = 150 \sin(\theta - \pi/6)$.
9.9 A single-phase cascaded multilevel inverter has $m = 5$. Find the generalized Fourier series and THD of the phase voltage. **(b)** Find the switching angles to eliminate 5th, 7th, 11th, and 13th harmonics.
9.10 A single-phase cascaded multilevel inverter has $m = 5$. **(a)** Find the generaiized Fourier series and THD of the phase voltage. **(b)** Find the switching angles to eliminate 5th, 7th, and 11th harmonics if the peak fundamental phase voltage is 60% of its maximum value.